SIEMENS

Ingenuity for life

Oasys-RTL

Physical RTL synthesis

Benefits

- Best quality of results achieved through optimization at RTL
- Handles 100+ million gates because of higher level of abstraction
- Runtimes up to 10x faster than traditional RTL synthesis
- Faster floorplan closure with the industry's only RTL-level floorplanning capabilities

Features

- Physically-aware RTL synthesis based on patented "PlaceFirst" technology
- Integrated cockpit for advanced cross probing between logical, physical, timing and other views
- Integrated links for formal equivalency checking
- Parallel design space exploration of PPA metrics
- Comprehensive power optimization and analysis capabilities

The Oasys-RTL™ physical RTL synthesis solution is a revolutionary advancement in the state-of-the-art synthesis technology. It addresses the limitations of traditional RTL synthesis tools that were designed decades ago.

Oasys-RTL has been architected to meet the needs of complex, advanced- node, high performance designs with the capacity to handle 100+ million gates and up to 10X shorter runtimes. Oasys-RTL integrates full chip-level physical synthesis, floorplanning, and optimization at a higher level to enable RTL designers to accurately identify and resolve timing, routability, and power issues early in the design cycle. Oasys-RTL's patented "PlaceFirst" synthesis technology enables optimization at the RTL level and delivers the best quality of results (QoR).

Oasys-RTL addresses the need for higher capacity, faster runtimes, improved QoR, and physical awareness by optimizing at a higher level of abstraction along with offering an integrated floorplanning and placement capabilities.

Best Quality of Results

Oasys-RTL's patented "PlaceFirst" technology integrates placement into the core synthesis algorithms as a primary cost function, thereby enabling high-level optimization similar to what modern compilers can do to software programs. Oasys-RTL's physical RTL synthesis works by partitioning the RTL into virtual placeable entities, and then refining those down into actual library cells so that there is always a full placement that goes with the timing values. In addition, Oasys-RTLworks with the full-chip global view of the design, and the effects of any physical changes are immediately propagated to the entire design to drive subsequent synthesis runs. This leads to reliable convergence and superior QoR. Oasys-RTL applies cutting edge global placement technologies in combination with global routing connectivity and congestion-aware algorithms to minimize congestion related to timing closure.

Oasys-RTL is thus able to deliver the QoR by addressing the limitation of the traditional synthesis tools that focus on

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very low, gate-level local optimizations that limit the QoR improvement opportunities or take a large number of small incremental computations to achieve acceptable results.

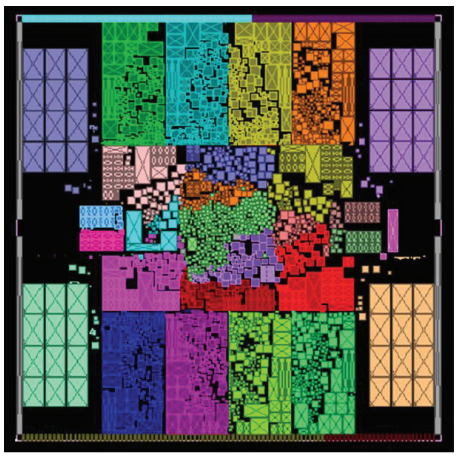
Highest Capacity and Fastest Runtime

Oasys-RTL has the ability to handle 100+ million gate designs with up to 10x faster runtime compared to traditional synthesis tools. The significant improvements in capacity and runtimes are primarily due to the higher level of abstractions – i.e. dealing with the design at virtual RTL objects (1000s') instead of gates (millions). The innovative architecture and data model significantly improve the memory utilization and runtimes. The large capacity and fast runtime of the Oasys-RTL shortens the synthesis task from days to hours.

Integrated Floorplanning

Oasys-RTL is the only solution on the market that combines physical RTL synthesis and RTL floorplanning into a single tool. RTL partitions are optimized concurrently for placement, timing, power, area, and congestion. Then macros, pins, and pads are automatically placed to come up with a high quality seed floorplan for the given constraints. It considers regions, fences, blockages, macro placement, density screens, and other physical guidance from the advanced floorplan editing tools for rapid floorplan and constraint refinement.

Using Oasys-RTL, RTL engineers can automatically generate a floorplan in a matter of days with minimal physical guidance. They can also identify timing and congestion issues before handing off the floorplan and a netlist to the back-end team. This handoff significantly increases the time to floorplan and design closure.



Automatically create a floorplan from RTL in a matter of days.

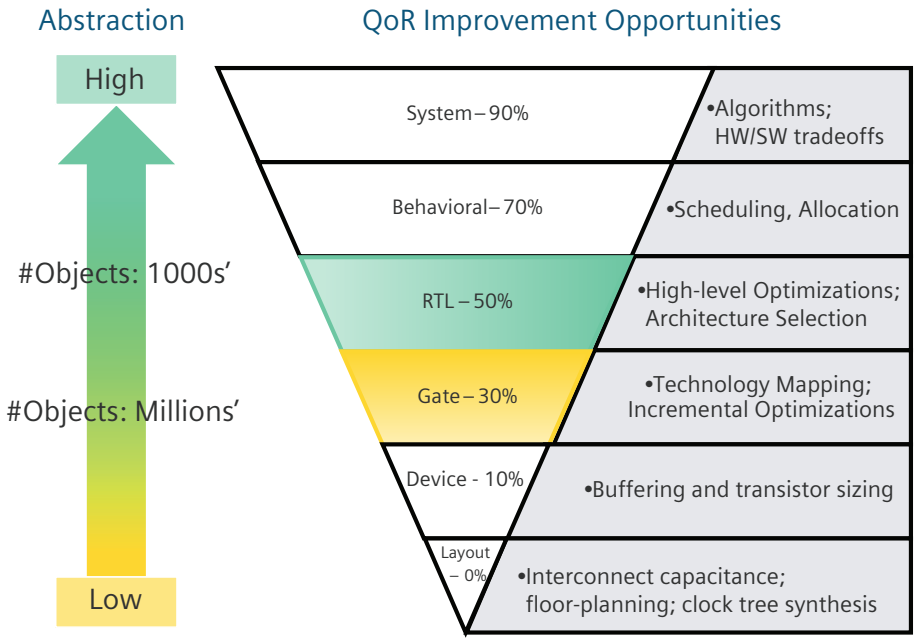
Congestion-Aware Synthesis

Oasys-RTL, engineered ground-up for physically driven synthesis, identifies and mitigates congestion during its optimizations using statistical, topological, partitioning, and placement-driven algorithms. Unlike traditional congestion minimization techniques that make use of micro gate-level transforms, Oasys-RTLoptimizes for congestion at the much higher RTL-level of abstraction, making use of its functional knowledge of the RTL and appropriate partitioning.

Power-Aware Synthesis

Oasys-RTL has a comprehensive suite of technologies for power-aware synthesis and also for power analysis to meet the power budgets of modern designs, including multi-threshold libraries, clock gating, and UPF based multi-VDD flows.

Oasys-RTL performs dynamic and static RTL power analysis, optimization, and debug. It can read in activity information from a VCD file or can be provided with a variable toggle rate for stimulus. Hotspots can be highlighted in the floorplan, and can be cross probed to the RTL to uncover the root cause of the issues.



RTL-level optimization enables higher capacity and faster runtimes.

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Integrated Cockpit

Oasys-RTL's powerful ability to cross-probe between the physical and RTL databases allows RTL engineers to quickly and accurately identify the root cause of timing and congestion issues and resolve the problems early in the design cycle. Oasys-RTL is the first tool to provide all the design views, from logical to physical to timing, in a single RTL synthesis platform.

Visualize and interact with the physical results of RTL synthesis. Cross- probing allows designers to make changes and re-run synthesis quickly.

Oasys-RTL also provides different physical views for early debug including static/dynamic power map, congestion map, critical timing map, and hierarchical floorplanning view.

Design Space Exploration

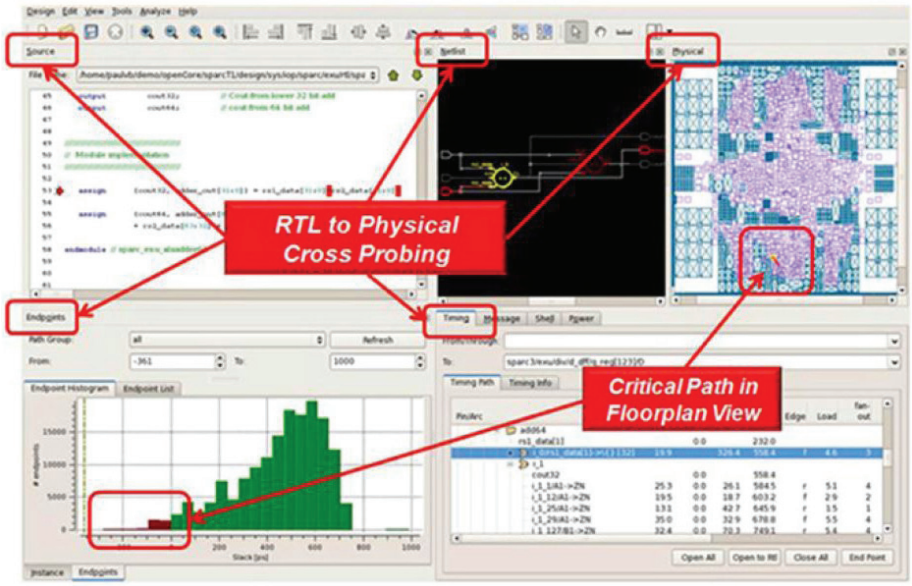
The capacity and speed of Oasys-RTL enables designers to perform parallel design space exploration of different design metrics such as power, performance, and area. Oasys-RTL's Parallel Implementation Exploration feature provides the ability to actively explore design alternatives prior to implementation.

Oasys-RTL can seamlessly do multiple synthesis runs by changing constraints of the design, such as voltage, clock speed, and the physical library, and then provide a comprehensive summary of results for comparison.

Oasys-RTL in the Flow

Oasys-RTL takes standard synthesis inputs and produces standard synthesis outputs along with placement information to guide and accelerate placement and routing tools.

- Inputs:
  - RTL (Verilog/VHDL/SystemVerilog)
  - Technology Library (LIB)
  - Physical Library (LEF)
  - Parasitics (RLC/xACT)
  - Timing Constraints (SDC)
  - Power (UPF)
  - DFT (CTL)
  - Floorplan (DEF)
- Outputs (Optional):
  - Gate-level netlist (Verilog)
  - Floorplan (DEF)
  - ScanDEF



Visualize and interact with the physical results of RTL synthesis. Cross- probing allows designers to make changes and re-run synthesis quickly.

Summary

Oasys-RTL represents a paradigm shift in the RTL synthesis domain with its unique physical RTL synthesis engine. Oasys-RTLdelivers up to 10x faster synthesis run times compared to traditional synthesis tools while also delivering optimal PPA metrics. Its unique scalable architecture provides 100+ million gate design capacity to tackle the growing design sizes with ease with a compact memory footprint.

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