

Questa ADMS

Analog-digital/mixed-signal verification

Features and benefits

Digital Verification for AMS

- SystemVerilog and UVM with mixed-signal extensions
- Effective functional verification in presence of analog signals
- Fast event-driven and real number verification modeling
- Accurate AMS verification modeling
- SVA applied to analog signals
- Familiar Questa debugging environment
- Analog coverage presented in UCDB
- UPF 2.0 with mixed-signal extensions

Digital Verification for AMS

- Analog testbenches applied to mixed-signal designs
- Effective corner analysis in presence of digital signals
- Familiar EZwave™ waveform display
- Visual debugging of current contributions
- Integrated with Siemens Pyxis™ Schematic and Cadence® Virtuoso® tools

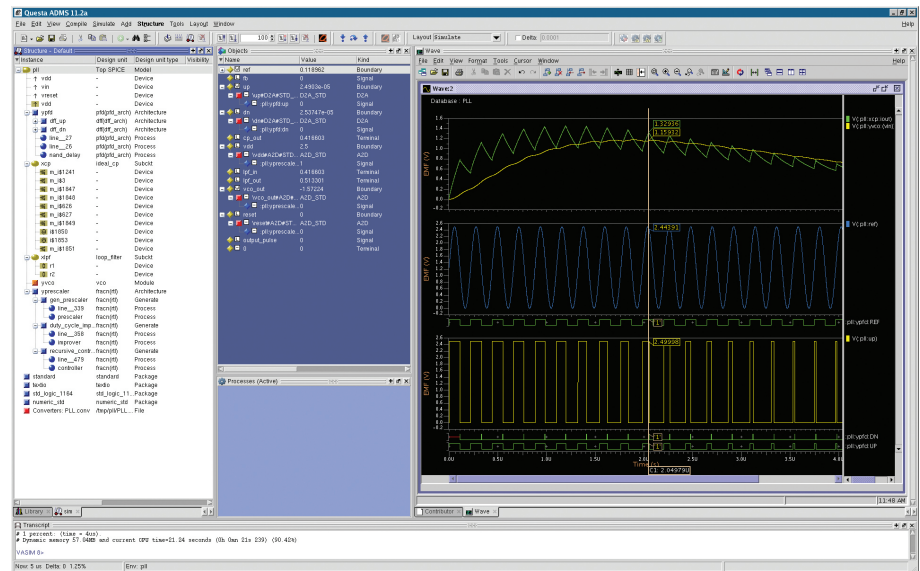
Questa® ADMS extends the Questa verification environment to include verification of circuits that contain analog IP. Digital verification engineers as well as analog designers use Questa ADMS to verify that complex analog and mixed-signal designs fulfill their requirements. Questa ADMS combines several high-performance simulation engines in one efficient tool. It supports every major hardware description language and exchange standard.

A flexible mixed-signal verification strategy

System-level verification of modern SoC designs that include analog blocks presents a challenging problem to the verification engineer. Each of the four primary AMS verification areas – functional, parametric, implementation, and reliability – demands a different set of time/accuracy trade-offs, verification models, and analog simulation engines.

Questa ADMS supports all three major methodologies for mixed-signal verification:

- Event-driven (usually Real Number) verification models that are simulated directly in a high-speed, event-driven digital engine for the fastest possible simulation



Questa ADMS is the de facto industry standard for the creation and verification of complex analog and mixed-signal designs.

Questa ADMS

- Continuous time AMS verification models for demanding analog applications where high accuracy is necessary, but SPICE level models are too slow
- Co-simulation between the digital RTL description and the analog SPICE design when use of verification models is not an option

Switching between these methodologies as the need arises for different test points or at different times in the design cycle is an important capability supported by the Questa ADMS verification solution.

Verification across the A-D boundary

Questa ADMS extends the advanced verification features familiar to digital designers to the mixed-signal world.

Design languages and exchange formats

The Questa ADMS environment is language neutral so VHDL-AMS, Verilog-AMS, VHDL, Verilog, SystemVerilog, SPICE, and SystemC can be combined in a single design. SPICE, VHDL, or SystemVerilog can be used at the testbench level. Questa ADMS supports both SDF, for back-annotation of timing data to digital library modules, and DSPF, for backannotation of parasitics in full customer design.

Questa ADMS supports the following languages and exchange formats:

- IEEE 1497 Standard Delay File Format (SDF)
- IEEE 1076.1 VHDL-AMS
- IEEE 1076 VHDL
- IEEE 1364 Verilog
- IEEE 1800 SystemVerilog
- IEEE 1666 SystemC
- IEEE 1801 UPF
- Accellera standard Verilog-AMS
- Accellera standard UVM
- Value Change Dump (VCD), read, and write

- Detailed Standard Parasitic Format (DSPF)
- SPICE Eldo, HSPICE, and Spectre® dialects

Verification language extensions

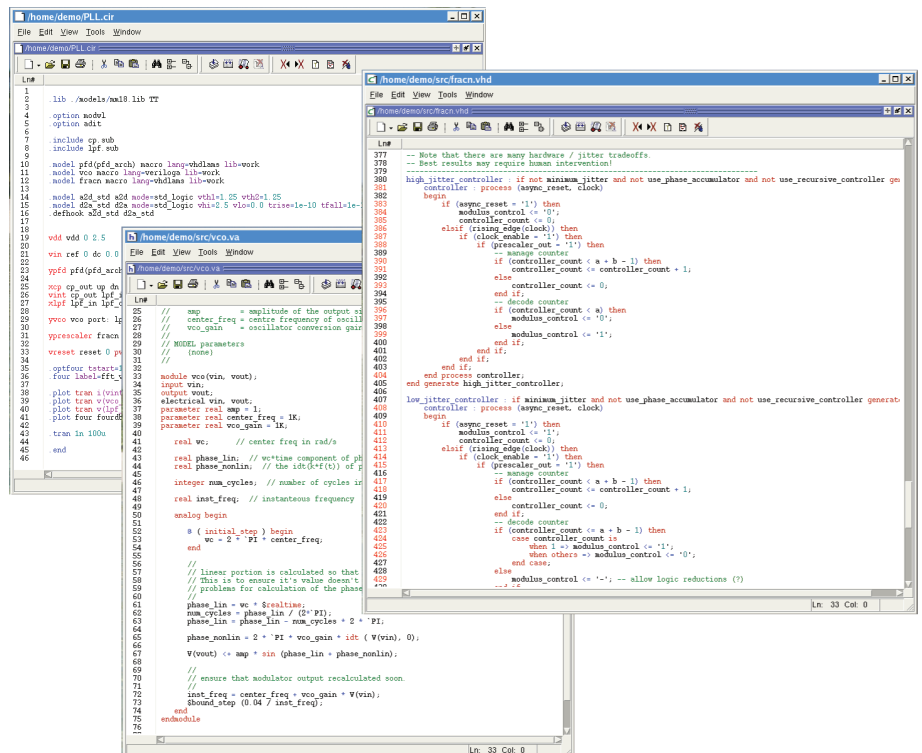
Questa ADMS provides enhanced HDL language coverage by extending Verilog-AMS with a complete implementation of the SystemVerilog assertion (SVA) sublanguage, making it possible to directly code analog assertions. The Questa ADMS SVA extension also allows relational operators on real values in expressions.

The verification engineer can use the SystemVerilog bind statement in a testbench to add a module to any digital or AMS context (including SPICE) inside Questa ADMS. Any connection between the digital ports of the bound module and the analog elements of the binding context are made through automatically

inserted connect modules, which may be user defined.

The bound module typically contains SVA statements and coverage statements. Since the insertion of connect modules is handled automatically, a single module can be bound to either a digital or an analog context to make the same measurement. The verification engineer can replace a digital DUT with its mixed-signal equivalent and leave the testbench unmodified. All assertion and coverage information is written to the Universal Coverage Database (UCDB) along with enough information to locate the results of a simulation and reproduce the run.

Support for wreal (wire-real) signals in Verilog-AMS and SystemVerilog allows engineers to code abstract analog models using event-driven simulation (sometimes called RN, or Real Number modeling) to speed full-system simulation.



In the Questa ADMS environment, various languages, such as VHDL-AMS, Verilog-AMS, VHDL, Verilog, SystemVerilog, SystemC, and SPICE, can be combined in a single design.

UVM and UPF extensions

Questa ADMS supports using the Universal Verification Methodology (UVM) with a mixed-signal design under test. A library of analog interface sources and probes extend the UVM for analog stimulus and measurement to the monitor/driver/responder level. These interface components range in complexity from the simplest voltage measurement and waveform generator to complex waveform extraction.

Mixed-signal extensions to the Unified Power Format (UPF) allow verification engineers to connect power supply pins to power supplies that are dynamically controlled by UPF power nets. Connect modules can be dynamically calibrated by the power nets of the power domain.

Configuring the design hierarchy

Configuration is the process of choosing the right version of a module or component for each element in the design hierarchy. System-level mixed-signal verification requires a large number of configurations and the ability to reconfigure rapidly and confidently.

In Questa ADMS, all languages can be mixed in a single hierarchy, and there are no restrictions on what language can go where. The testbench can be SPICE, an analog or mixed-signal language, or a digital language. Digital parts simulated by Questa can be used in Questa ADMS without any modification. SPICE sub-circuits can be used anywhere in the design hierarchy for greater flexibility in modeling. For example, SPICE can instantiate SystemVerilog, and SystemVerilog can instantiate SPICE.

Both Verilog and VHDL configuration declarations can be used to build a design hierarchy with a language on top. SPICE-ontop configuration is easy with the Questa ADMS binding command language. Configuration includes replacing a digital block by an analog or mixed-signal block, or vice versa. There is a mixed-signal net wherever an analog signal connects to a digital signal,

and every mixed-signal net requires a digital/analog connect module: A-to-D, D-to-A, or bidirectional.

Inserting connect modules is taken care of automatically by Questa ADMS, following instructions supplied in the command file. The instructions can be general or specific, even down to specifying the boundary of a single net. Designers can choose among built-in connect modules or design their own in VHDL-AMS or Verilog-AMS. The digital side of a boundary can be any supported net type, including VHDL records. Connect modules can be connected to UPF or SPICE global power supplies for power-aware designs.

The command file containing boundary information is separate from the design hierarchy itself, so there is no need to code boundary placement into the digital portions of a design. Digital designers remain unconcerned about voltage island or power issues. The "golden" RTL netlist can be left undisturbed during subsequent system verification runs that include analog blocks. Questa

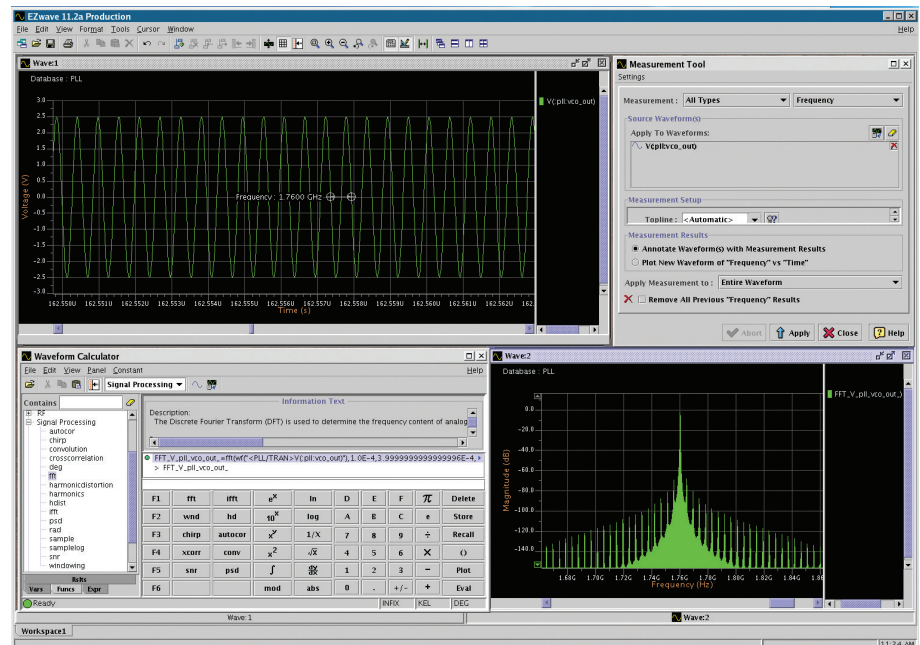
ADMS also supports the standard Verilog-AMS connect module methodology.

EZwave Waveform Processor

Questa ADMS offers the EZwave™ waveform processor to supplement the standard Questa viewer. EZwave provides the additional features necessary to display and analyze a mixture of RF, low-frequency baseband analog, and digital signals. It manipulates data in both the frequency and time domains. Smith charts, eye diagrams, FFT with sophisticated windowing, or signal-to-noise calculation are just some of the built-in features.

Integration in standard design flows

Questa ADMS provides a stand-alone flow that extends the familiar Questa environment for integrated mixed-signal model development and simulation. New dynamically linked debugging and design visualization extensions help to pinpoint problems in mixed-signal designs. The Questa power-aware flow and digital optimizer work smoothly in



Questa ADMS with the EZwave waveform processor allows displaying and analyzing RF, low-frequency baseband analog, and digital signals.

Questa ADMS. Questa ADMS supports the SystemVerilog UVM for complex system verification. The integrated TCL scripting language enables batch control of the simulation and waveform display.

Pyxis schematic

Questa ADMS integrates with the Pyxis™ Schematic tool by combining flexible model registration and selection with the Pyxis Schematic simulation cockpit and the high-speed hierarchical netlister. A complete simulation interface in Pyxis Schematic controls the simulation set up and the netlisting process.

Cadence Virtuoso analog design environment

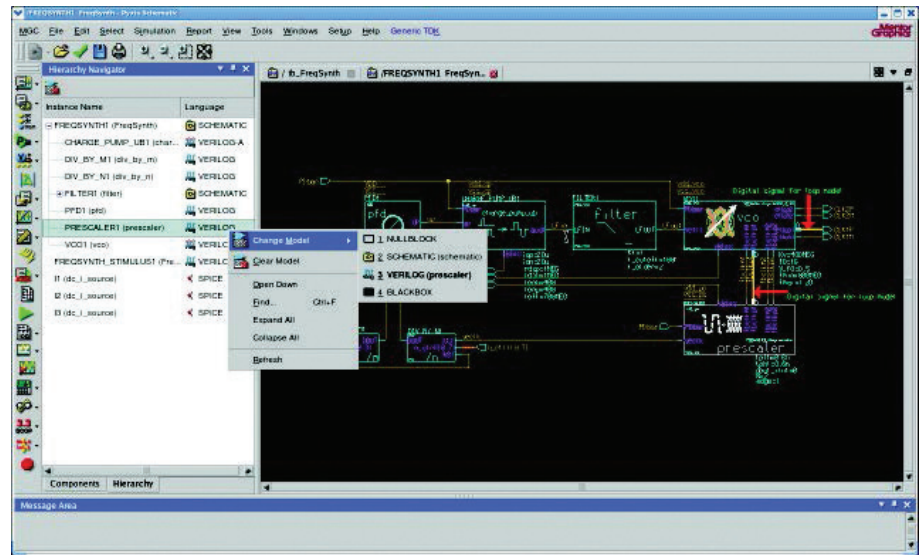
Questa ADMS integrates with the Cadence Virtuoso® analog design environment using the same look and feel as a native simulator while providing the advantages of Questa ADMS analysis, commands, and options. An enhanced symbol library that provides specific Eldo devices is compatible with the Cadence library. Legacy models coded in the Spectre SPICE dialect can be used without alteration. Simulation setup, direct netlisting, waveform processing, and cross-probing are fully supported.

HyperLynx analog

Questa ADMS is the simulation engine underlying Siemens HyperLynx® Analog for functional verification of complete printed circuit boards. A single schematic supports both PCB layout and functional analysis. HyperLynx Analog combines with HyperLynx Signal Integrity to extract parasitic PCB trace models for comprehensive board-level functional analysis.

EDA Simulator Link MQ

EDA Simulator Link™ MQ (The MathWorks, Inc.) is a co-simulation interface that provides a bidirectional link between MATLAB™ and Simulink® and Questa ADMS. It provides native



Questa ADMS integrates with the Pyxis Schematic simulation interface to control the simulation set up and netlisting process.

co-simulation support for both VHDL and SystemVerilog. The traditional Simulink system-level design and simulation environment supports mixed-language simulation of MATLAB, C, C++, and Simulink blocks. By adding hardware design languages to the mix, EDA Simulator Link MQ integrates algorithm and system design with hardware implementation.

Simulation engines

Questa ADMS provides all the advantages of digital, analog, and mixed-signal standard HDLs and SPICE in a unified simulation environment. Questa ADMS incorporates five customer-proven Siemens simulation engines.

Questa

Questa combines high performance and high capacity with the code coverage and debugging capabilities required to simulate larger blocks and systems. Comprehensive support of SystemVerilog, VHDL, and SystemC provides a solid foundation for single and multilanguage design verification environments.

Eldo Classic

The Eldo Classic analog kernel is the simulator of choice for IC silicon vendors and fabless design houses. Eldo Classic has been used to verify and successfully fabricate thousands of ICs. It is the absolute, golden, sign-off reference for verification engineers and designers on three continents. This loyalty is the result of a continuing investment of Siemens' engineering talent, patience, and commitment.

Eldo Premier

Eldo Premier is an accelerated transistor-level time-domain simulator that uses sophisticated resolution techniques to accelerate the transient simulation of very large and CPU-intensive circuits without sacrificing accuracy. With the same use model as Eldo Classic, Eldo Premier can easily be integrated into an existing customer signoff flow, yet it offers a 2.5 to 20x speed-up and 10x capacity over traditional SPICE simulators. Hundreds of industry test cases have been used to validate the technology and results and compare favorably to the "golden" simulation results from Eldo Classic.

ADiT

ADiT is a Fast-SPICE simulation engine targeting analog and mixed-signal (AMS) transistor-level applications. ADiT was designed specifically for analog and mixed-signal circuits that demand high accuracy. ADiT features a mixed-signal-aware partitioning algorithm that allows fast and accurate simulation of circuits with non-ideal power supplies. It embeds charge-conserving analytical and table-based device modes to deliver accurate, reliable results 10X to 100X faster than traditional SPICE simulation.

Eldo RF

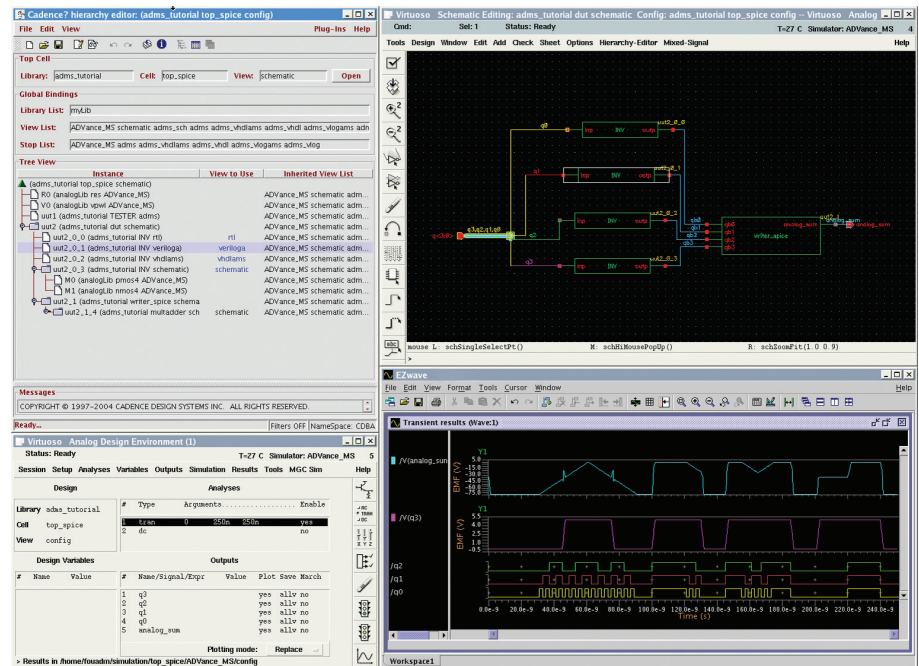
Eldo RF targets digital communication systems that include tightly integrated RF along with analog mixed-signal and DSP functions. The Eldo RF MODSST algorithm works with descriptions using any mix of simulation languages. It uses a mixed time-frequency algorithm that computes a time-varying spectrum. The spacing of time points is chosen to follow the slow-varying baseband information, rather than the fast-varying RF carriers. The results have the same accuracy as tedious circuit-level transient simulation.

Speeding up mixed-signal simulation

Simulator performance is important when working against a deadline, but performance is not enough. Questa ADMS offers intelligent control features that yield aggregated simulation throughput at multiples of raw simulation speed.

Multiple run simulations

Questa ADMS will distribute multiple runs in parallel on the processors of a single machine or over a networked compute farm. Multiple run distribution can be used for parameter step and Monte Carlo simulations. The mechanism is fully compatible with load balancing tools such as LSF or Sun Grid and even with proprietary dispatching tools. Because the simulations run entirely in parallel, productivity scales linearly with the number of CPUs available.



Questa ADMS integrates with the Cadence Virtuoso Analog Design Environment using the same look and feel as a native simulator.

Checkpoint and restart

Questa ADMS allows the designer to save a checkpoint image of an ongoing simulation at any time. Then later, the same simulation can be restarted on the same or a different machine. It is even possible to change parameters before restart or to present a different set of test vectors to the restarted simulation. A single simulation can be executed until initialization is complete, and then the checkpoint image can be restarted any number of times. By factoring out redundant initialization, better verification coverage yields are attainable when working against a deadline.

Scalable multi-threading performance

Questa ADMS can simultaneously use all processors on a multicore computer for computations at the device level. Through the Eldo Premier simulator's optimized, natively parallel and scalable code, it takes maximum advantage of multicore machines, accelerating single-thread and multi-thread simulations. The acceleration of single-thread

simulation is accomplished by algebraic techniques for the resolution of a system of non-linear differential equations. The acceleration of multi-threaded simulations is achieved by the natively parallel code of the simulation kernel and its dedicated data structures. Eldo Premier multi-threads the entire matrix solution and device evaluation. Speed is also scalable, with speed-up factors of three times or more on four cores and up to six to seven times on eight cores.

Digital initialization for mixed-signal

It can take up to a millisecond or more of simulation time to initialize the digital state machine of a complex mixed-signal model. That can eat hundreds of thousands of simulation cycles. But signals from the analog portions of the design are often actively suppressed or passively ignored until digital initialization is complete. Questa ADMS offers the unique ability to delay the startup of analog simulation until the testbench signals that the digital initialization is complete. The improvement in

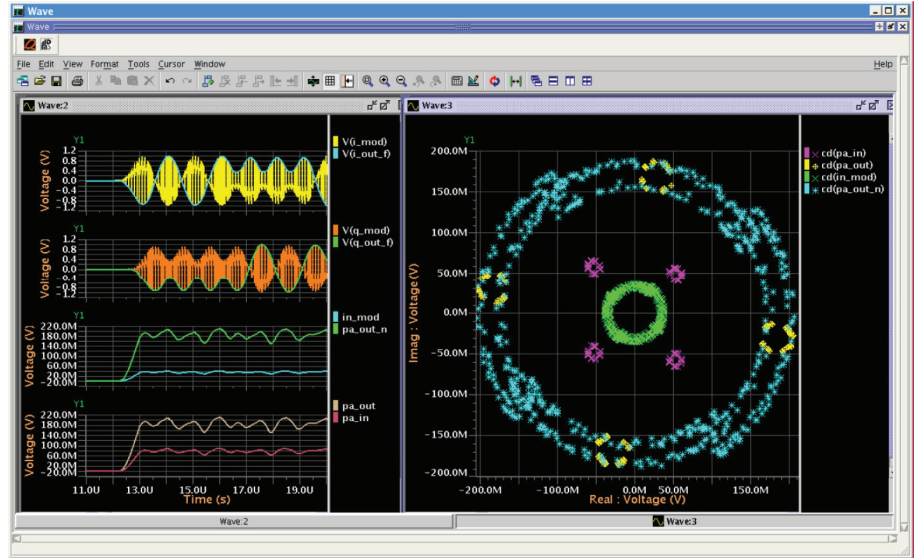
performance during startup can be one or two orders of magnitude.

Dynamic programmable accuracy control

Analog simulation speed is strongly dependent on the accuracy and frequency of the calculations required to solve the equations that represent the model. A complex sequence of tests will exercise different portions of the analog content of a design at different times. Questa ADMS allows the designer's test-bench to dynamically change the time step and convergence criteria at a given simulation time and for a particular sub-circuit. Then, once the test is complete, the accuracy controls can be relaxed to speed simulation.

RF verification with mixed time-frequency algorithms

Many digital communication systems integrate an RF front-end together with complex baseband digital signal processing. Verifying systems such as direct conversion receivers or automatic gain control loops requires a simulator that can handle the transistor-level RF part simultaneously with the baseband part – and do it against a deadline. Questa ADMS delivers improvements of two or three orders of magnitude over less agile simulators when tested on mixed-signal RF designs with typical baseband-to-carrier frequency ratios.

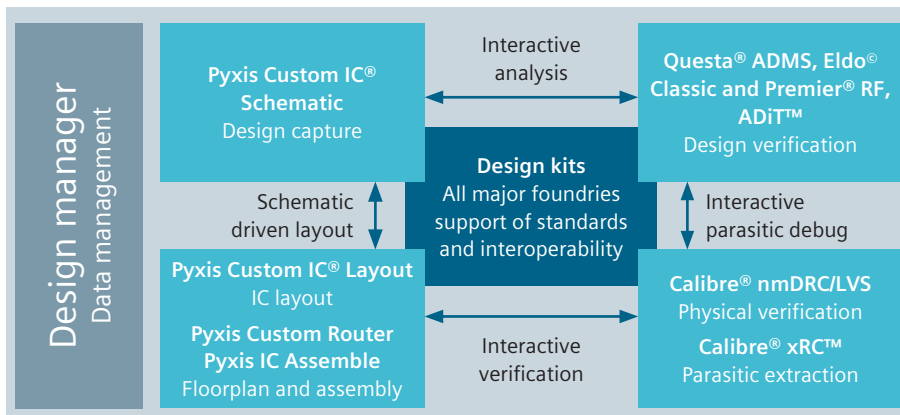


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Fast development of AMS models

Behavioral models in the AMS languages are an indispensable weapon in the mixed-signal verification arsenal, but AMS language modeling can be time-consuming. The interactive AMS Modeling Cookbook for VHDL-AMS and Verilog-A combines techniques for mixed-signal behavioral modeling that give the mixed-signal modeler a vital head start. The example models cover a variety of communications and multimedia applications. They can be used out-of-the-box for system level design,

architectural exploration, system level functional verification, and for enhancing the simulation speed of complex mixed-signal systems. The AMS Modeling Cookbook serves as a ready source of modeling templates, tips, and techniques for developing customized, efficient, and accurate behavioral models. Every model is extensively documented to make it easy to reuse. All the source code is included. Multiple hot-linked indexes make reference easy; clicking on a model name from any index links directly to the documentation and source code.



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