

DIGITAL INDUSTRIES SOFTWARE

# Precision<sup>®</sup> RTL

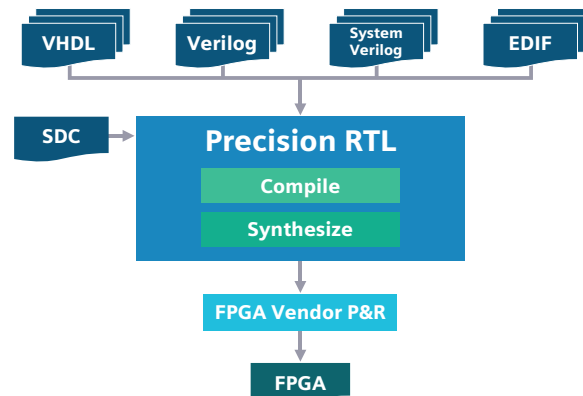
Advanced FPGA Synthesis Technologies

## Benefits

- FPGA vendor independent synthesis
- Excellent quality of results
- Industry leading language support for Verilog, VHDL, SystemVerilog
- Award-winning design analysis
- Precise-IP™ - FPGA vendor independent IP platform
- Unique integration between synthesis and Siemens FPGA tools

## Summary

Precision RTL, Siemens entry-level FPGA synthesis product, offers best-in-class quality of results with a vendor-independent FPGA synthesis solution. It is tightly integrated with FormalPro LEC for equivalency checking and HDL Designer for design capture and design verification using ModelSim/Questa.



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**Industry-leading FPGA synthesis**

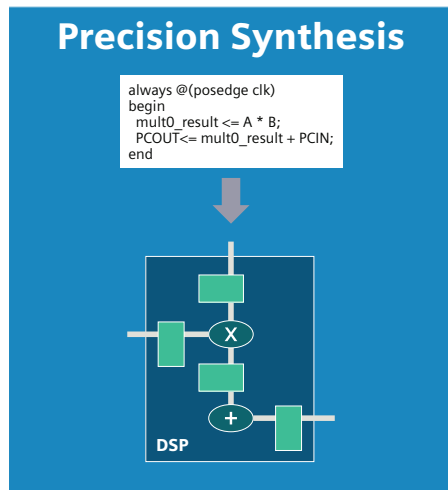
With a rich feature set that includes advanced optimizations, award-winning analysis, and industry-leading language support, Precision RTL enables vendor-independent design, accelerates time to market, eliminates design defects, and delivers superior quality of results.

**FPGA vendor independent synthesis**

Precision RTL synthesis allows you to target across multiple FPGA vendors such as AMD (Xilinx), Intel (Altera), Microchip (Microsemi) or Lattice. Designers may use the same HDL and constraint inputs for any vendor/ device. This enables you to choose the best device for your design based on performance, area, power and price.

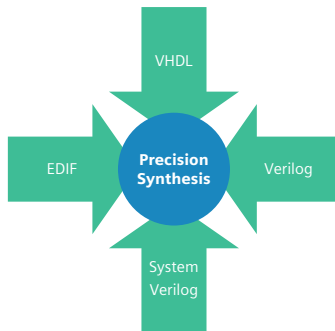
**Excellent quality of results**

Meet performance goals quickly with Precision RTL’s advanced optimizations. Precision has been tuned to each vendor’s FPGA architecture and device resources. Users can achieve best-in-class performance and area through Precision’s effective utilization of DSPs, RAMs, shift registers & carry chains.



**Industry leading language support**

Precision RTL is an industry-leader offering the broadest coverage of HDL language support among the FPGA synthesis tools. Designers may use any combination of Verilog, VHDL, SystemVerilog, and EDIF languages. It supports timing constraints in the SDC (Synopsys Design Constraint) format used in FPGA designs.



**Award-winning design analysis**

Precision RTL’s award-winning design tools include RTL and gate-level technology schematics and reports to understand the post-synthesis results. It also allows designers to cross-probe from generated reports, to the post-synthesis technology schematic, to the generic RTL schematic, up to the relevant HDL code to understand all issues in their appropriate contexts. With Precision’s unique interactive static-timing engine it is very easy to perform “what-if” timing analysis for constraint refinement before running FPGA vendor place-and-route.

**Precise-IP™: FPGA vendor independent IP Platform**

As part of a complete FPGA vendor independent methodology, Precision RTL features Precise-IP™, a platform allowing designers to generate a wide selection of pre-verified IP for superior quality of results (QoR) across diverse FPGA families. In addition, Precision has partnered with leading IP vendors to offer a wide selection of cores validated for use with Precision Synthesis.

**Integration with Siemens FPGA design tools**

Siemens EDA has the only complete FPGA design flow in the industry with Precision in the center. It has tight integration with the following flows:

- High-Level Synthesis with Catapult®
- Design reuse with HDL Designer
- Equivalence checking with FormalPro®
- Requirements tracking with ReqTracer
- FPGA-PCB co-design with I/O Optimizer

**Part of the Precision Synthesis family**

Siemens offers three unique FPGA synthesis solutions. Precision RTL, Siemens’ entry-level FPGA synthesis product, offers best-in-class quality of results with a vendor-independent FPGA synthesis solution. Precision RTL Plus, adds DO-254 certification utilities for mil-aero applications, on-chip debug & validation and resource optimization for DSPs & RAMs. Precision Hi-Rel, enhances Precision RTL Plus with automated mitigation of SEUs/SETs in safety-critical & high-reliability applications using TMR, safe FSM and other optimizations.

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For additional numbers, click [here](#).