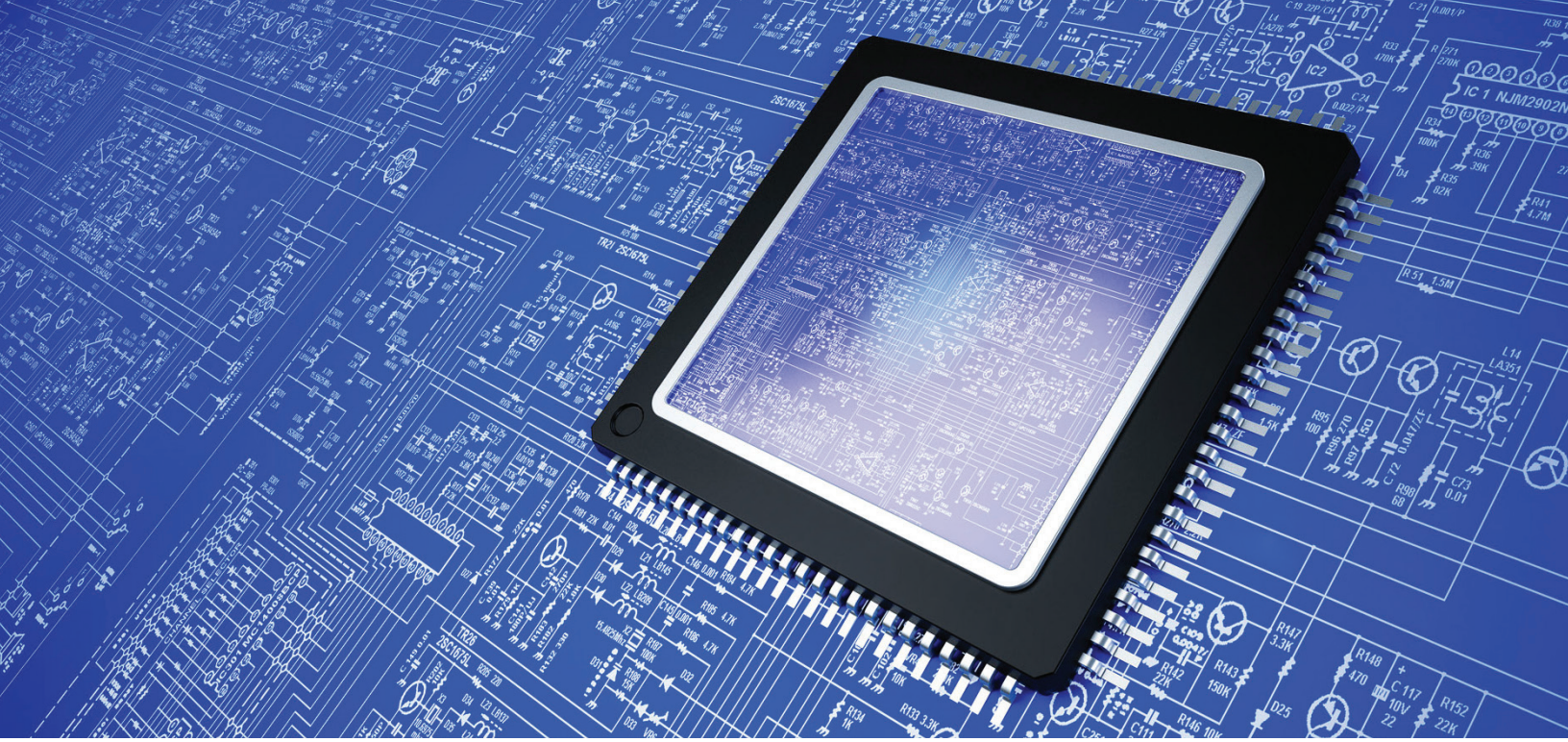

DIGITAL INDUSTRIES SOFTWARE

Tessent Diagnosis

From test results to root cause

Benefits

- Accelerates failure analysis by effectively classifying and localizing defects that can cause manufacturing test failures
- Enables a diagnosis-driven yield analysis flow
- Speeds up debug of timing-sensitive features
- Increases diagnosis resolution with incremental pattern generation
- Supports hierarchical DFT flows
- Correlates results with critical features identified by Calibre®

Accurately identify defects and timing errors

ICs developed at advanced technology nodes exhibit increased sensitivity to manufacturing variations. A small variation in process will affect layout features, creating defects in the chip that can slow yield ramp and lower mature yields. Investigating these types of defects can take weeks or months of effort in the failure analysis (FA) laboratory.

Tessent™ Diagnosis is the market-leading scan diagnosis solution, providing the highest accuracy rate. On average more than 80% of reports generated using Tessent Diagnosis have been confirmed using an FA process. Tessent Diagnosis results have been used to ramp yield across multiple nodes.

By correlating design information and failure data from manufacturing test with patterns from Tessent ATPG, Tessent Diagnosis turns failing test cycles into valuable data. Using layout-aware and cell-aware technology, it determines the defect's most probable failure mechanism, logic location and physical location. This detailed analysis of devices that fail manufacturing test greatly reduces the failure analysis effort and creates the foundation for diagnosis-driven yield analysis.

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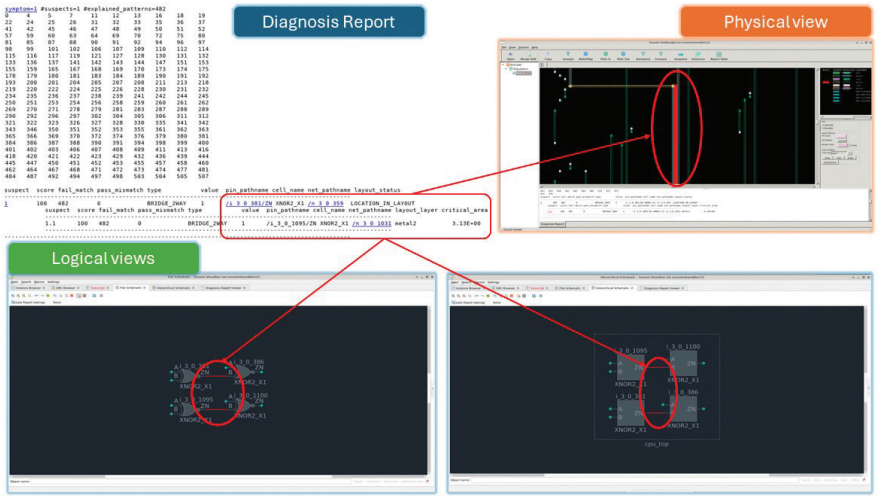
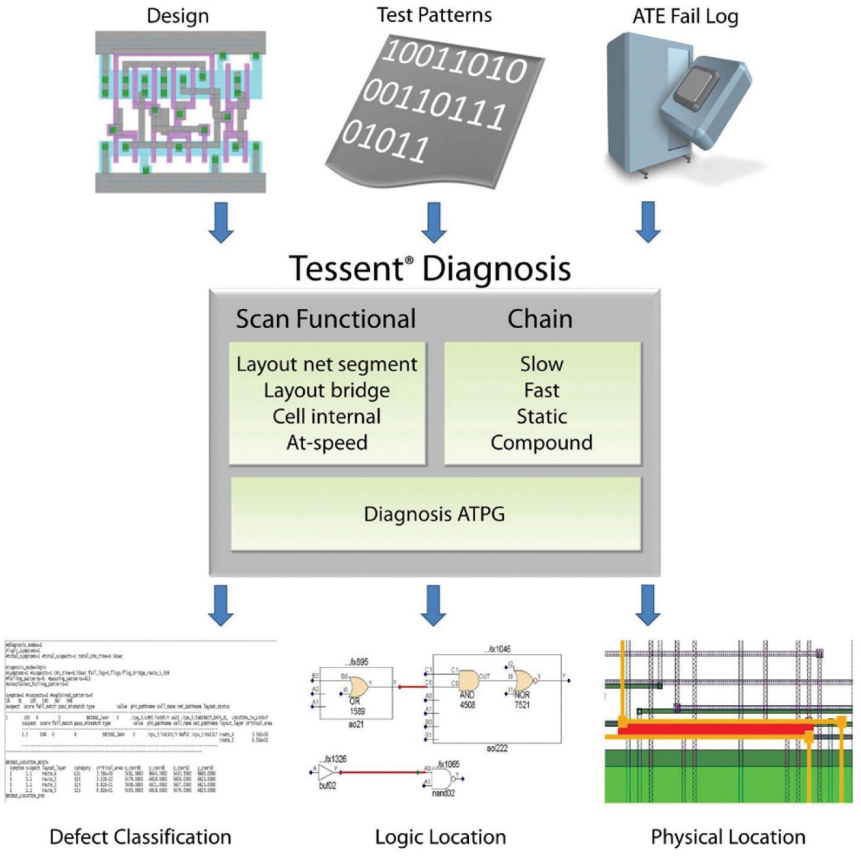
Features

- Accurate layout-aware diagnosis results and physical callouts
- Automated fail log monitoring and high-throughput distributed processing
- Scan chain diagnosis: cell, in, out, fast, slow
- Scan functional diagnosis: stuck, open, bridge, cell
- At-speed scan functional diagnosis: slow-to-rise, slow-to-fall, slow
- Optional cell-aware diagnosis provides transistor-level diagnosis
- Optional Hi-Res Chain for advanced process nodes (5nm and below)
- Direct diagnosis of Tessent TestKompress compressed test results
- Ranked and scored suspect list
- Separation of multiple defects



The Tessent Diagnosis solution identifies the type and location of defects, establishing the foundation for diagnosis-driven yield and failure analysis.

Tessent Diagnosis provides diagnosis-specific automatic test pattern generation (ATPG) algorithms to accelerate the FA process. Based on initial diagnosis results, additional patterns are generated to further improve diagnosis resolution.



The Tessent Diagnosis solution dramatically improves failure analysis.

Diagnosis results can be correlated with design-for-manufacturing (DFM) analysis results to identify critical design features. Tessent Diagnosis can read result databases (RDB) from Calibre® Pattern Matching and Calibre® YieldAnalyzer.

Tessent Diagnosis facilitates the diagnosis of production test patterns by directly accepting either compressed patterns from Tessent TestKompress or standard ATPG patterns from Tessent FastScan. The solution includes a server mode of operation to automate the process of diagnosing large volumes of failing die.

Advanced capabilities handle all major defects

Tessent Diagnosis handles all major defect mechanisms. The advanced scan chain diagnosis capability handles composite defects that affect chain and functional operation. This diagnosis for broken scan chains outperforms traditional methods in accuracy, resolution and suspects. Both intermittent and unmodeled defects are diagnosed.

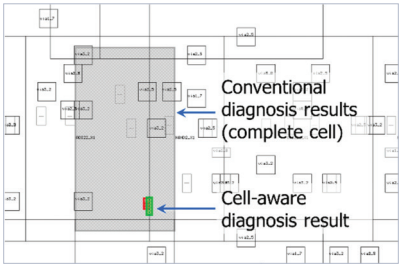
The layout-aware capability dramatically improves diagnosis resolution by analyzing the net topology of the suspect segment and eliminating false bridge and open defect suspects. The reduced suspect area accelerates FA, and the physical call-outs provide valuable classification for statistical analysis of diagnosis results. Physical design information in industry-standard LEF/DEF format is required.

The cell-aware diagnosis capability performs transistor-level diagnosis to identify defects inside standard cells. This capability leverages the same cell-aware fault model used for cell-aware ATPG and works with any pattern type (stuck-at, transition delay, cell-aware, etc.).

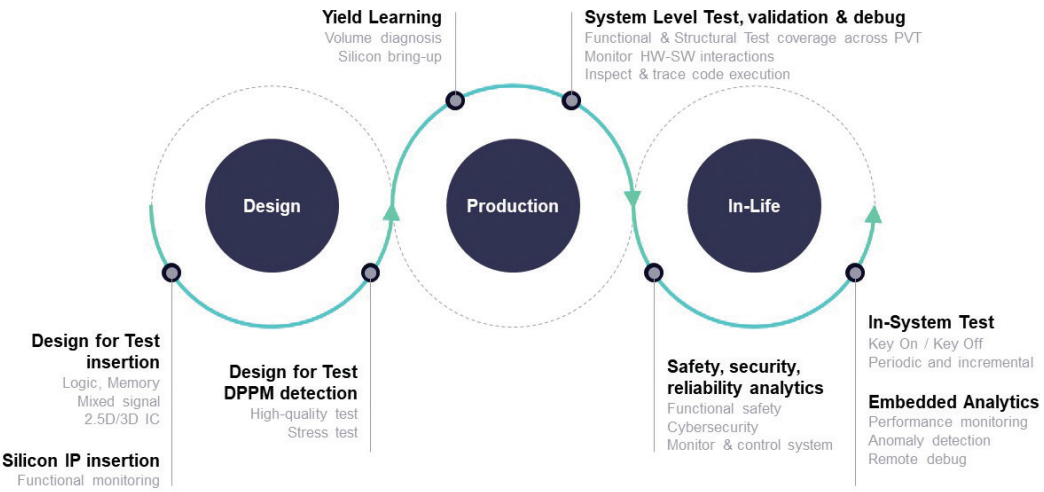
Tessent Hi-Res Chain Diagnosis, an option to Tessent Diagnosis, provides accurate transistor-level isolation for scan-chain defects. On advanced process nodes like 5nm and below, where yield ramp relies on chain diagnosis, this capability can improve the diagnosis resolution by >1.5X. This resolution savings can lead to FA avoidance, saving the semiconductor design company millions of dollars per product.

Tessent Product Family

Solutions for IC test and functional monitoring, including best-in-class design-for-test tools and test data analytics, security, debug and in-life monitoring products that help ensure the highest test coverage, accelerate yield ramp and improve quality and reliability across the silicon lifecycle.



Addressing IC lifecycle challenges with Tessent Silicon Lifecycle Solutions



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