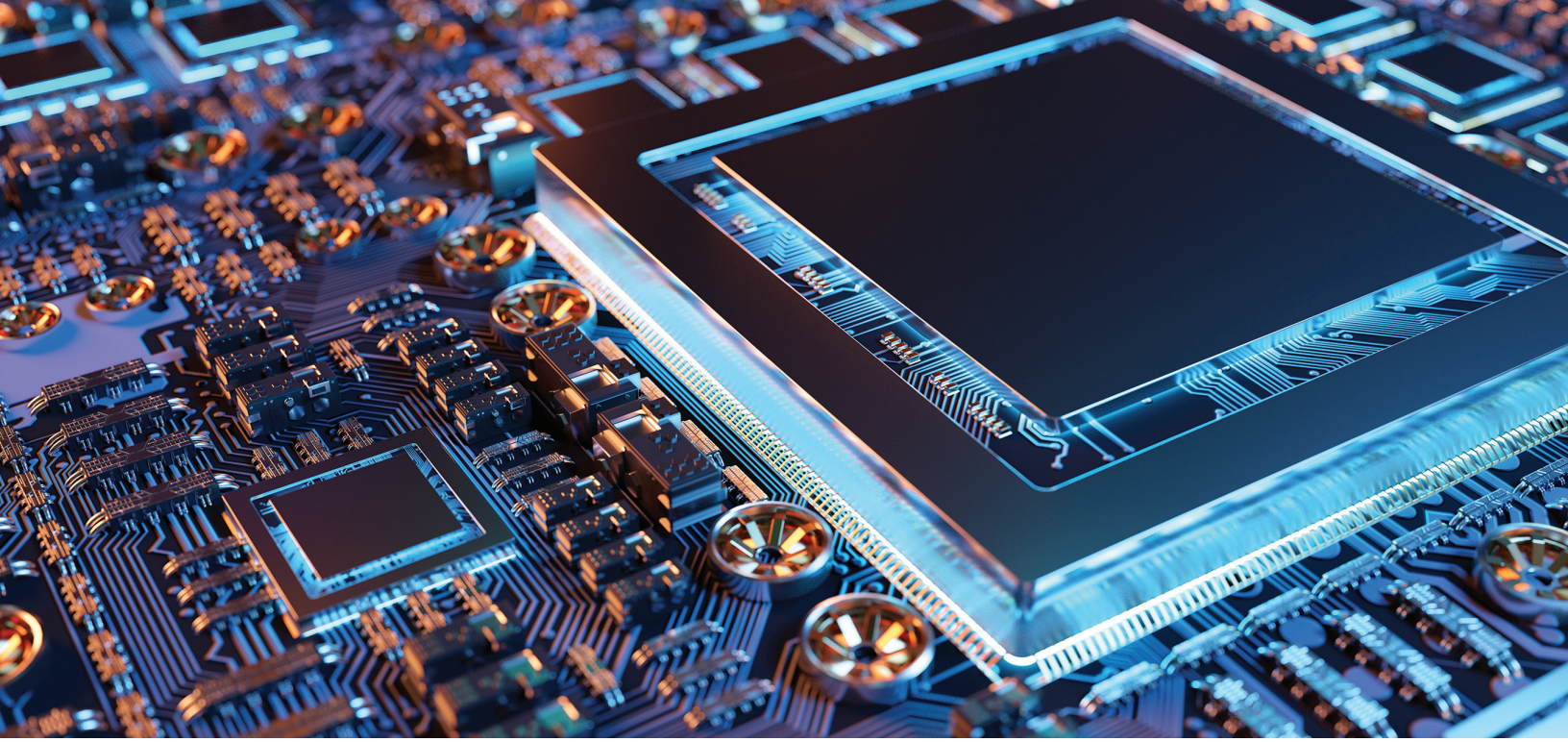


DIGITAL INDUSTRIES SOFTWARE

PowerPro Low-Power

Siemens Digital Industries Software Low-Power RTL Design Platform

Benefits

- A complete low-power RTL design platform offering power analysis and optimization capabilities in a single framework
- Fastest time-to-power for extremely large designs using fast incremental pseudo synthesis and parallel power computation that relies on a low-memory multi-cpu architecture
- Accurate RTL power estimation using inbuilt prototype synthesis engine within 15 percent of signoff
- Support for both averaged- and time-based power with ability to perform moving window

Low-Power RTL Design Platform

PowerPro is the leading low-power RTL design platform that helps create IPs/SOCs that are energy efficient by combining fast and accurate power estimation with industry's leading power optimization.

PowerPro helps deliver low-power, energy efficient designs by focussing on power very early on in the RTL design cycle. PowerPro's early power checking helps find power problems even when the stimuli is not available.

With the availability of functional stimuli, it helps find functionally redundant toggles in the design that waste power and allow the RTL designers to root-cause such toggles and gate their sources.

With the help of its physically aware RTL power estimation, it helps RTL designers evaluate if the design will meet power budgets. It is also tightly integrated with Siemens EDA's Veloce/Strato Hardware Acceleration platforms to enable system-level power estimation.

PowerPro's industry leading sequential optimization reports and ranks power saving opportunities for flops and memories that can be implemented quickly and easily to save power.

Benefits *continued*

- Analysis at multiple resolutions over peak power
- Advanced power linter allowing early power checking without need for stimuli or libraries
- Industry leading power optimization solution to guide low-power RTL design
- Push-button automatic low-power RTL generation with full formal verification
- Integrated with Siemens EDA's Veloce/ Strato emulation platform for power estimation in live and offline mode, for ultra large SOCs
- Integrated with Siemens EDA's Catapult High-Level Synthesis for achieving "C-to-low-power RTL synthesis"

PowerPro also offers industry's only automatic low-power RTL generation capability that is integrated with formal verification.

Fastest time-to-power

PowerPro's incremental power analysis flow lets designs to be compiled once and re-used multiple times with different stimuli. Under-the-hood, there is a multi-cpu architecture that relies on low-memory jobs to compute power in parallel. The combination of incremental run and highly parallelized power computation delivers extremely fast results.

Accurate power estimation

PowerPro utilizes Oasys synthesis under-the-hood to build a prototype of the design which coupled with physical awareness, provides accurate, out-of-the-box RTL-level power estimation that is within 15 percent of signoff.

PowerPro also has an inbuilt power aware reconstruction engine that captures temporal correlation for input stimuli for enhanced accuracy.

Both averaged and time-based power analysis is supported. With time-based power analysis, PowerPro computes peak power and also offers moving window average analysis that can be reconfigured to different resolutions to uncover power issues.

PowerPro also supports gate-level power estimation that is within 2-5 percent of signoff. RTL stimuli can also be used to compute power for gate-level designs.

Multiple input stimuli like FSDB, QWAVE and SAIF coming from either simulator or emulator are supported.

Power debug and visualization

PowerPro utilizes Siemens EDA's Visualizer Debug Environment that offers powerful features for visualization. Reports can be generated, sorted, filtered and cross-probed to RTL, schematic or waveform to identify power hotspots in the design. Cross-probing and comparison can be performed between physical information and design objects to discover potential power issues and fix them upfront.

PowerPro also offers the powerleaks flow where redundant toggles that waste power are marked on the waveform with all critical signals automatically loaded. RTL designers can root-cause the source of redundant toggles and fix them easily by cross-probing the waveform to RTL or schematic.

Early power checking

Power is most significantly impacted earlier in the design cycle. PowerPro's early power checking helps identify functional and structural redundancies in the design around flops, memories and CGICs at the RTL level without the need for input stimuli. PowerPro's power linting is well suited for regression where power issues can be found during early phases of RTL design and quickly fixed.

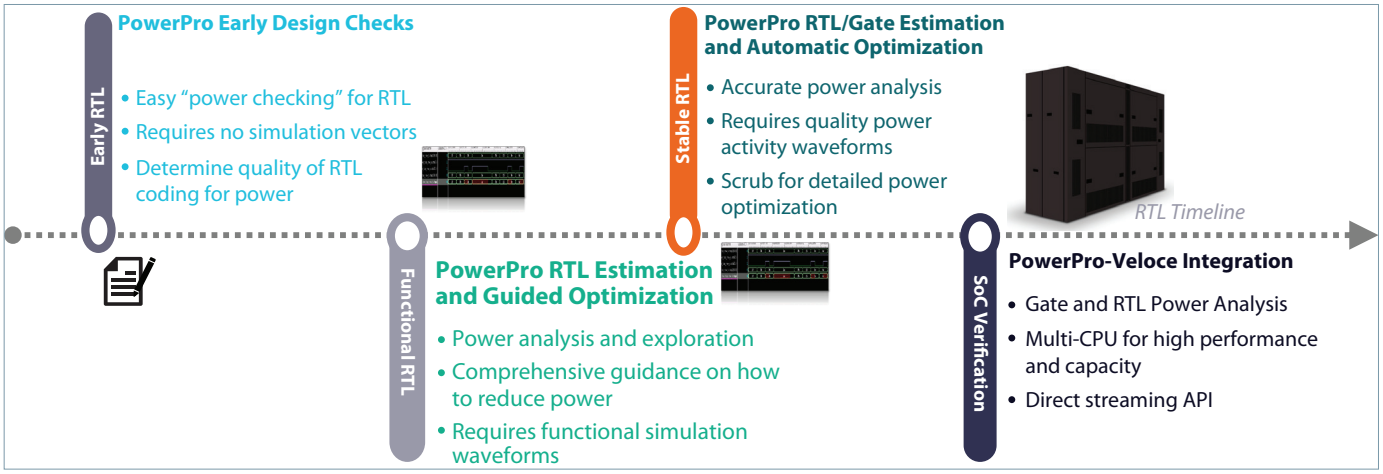
Power optimization

PowerPro's industry leading sequential power optimization finds clock gating and memory gating opportunities in the design through multi-cycle analysis that yields the highest power reduction with minimal area penalty and complexity. PowerPro reports complete enable expressions that the RTL designer can implement to save power with all the relevant information to do so. It also shows the RTL and logic equivalent of the enable expression for reference.

RTL designers can sort and filter the power saving opportunities on the basis of numerous factors such as power saving potential, combinational depth, hierarchical levels, etc. Sequential analysis engine can be pre-configured to report enable expressions that are simpler by constraining the various parameters of the analysis.

PowerPro's automatic power optimization flow generates the power optimized RTL automatically. The automatically generated low-power RTL maintains the indentation of the original RTL to maintain its readability. PowerPro's SLEC-Pro formal verification can be used with PowerPro to formally verify the machine generated RTL for equivalence.

PowerPro supports an ECO flow to accommodate late-stage functional changes in the design. The ECO flow allows users to generate directives to invalidate enables in the gate-level netlist.



Power qualification
PowerPro reports a large number of useful power metrics that can be employed to generate the power profile of an IP.

Metrics can be configured to set target values that act as key performance indicators for power. By defining the KPIs for power, IPs can be qualified and ranked accordingly.

A metrics driven regression framework can help track and trend metrics that are important for power for each RTL revision in an automated environment.

Emulation driven power analysis
PowerPro's integration with Siemens EDA's Strato/Veloce emulation platform means that power can be estimated at the system level. PowerPro supports both live mode and offline mode of power estimation.

Both averaged and peak power analysis are supported. With emulation, power can be computed for designs that are extremely large with extremely long simulation traces. This is enabled through inbuilt parallelization to handle both capacity and performance using multiple CPUs.

Integrated to Siemens EDA's Catapult High-Level Synthesis
Siemens EDA's flagship Catapult High-level Synthesis is integrated with PowerPro to help generate low-power RTL from C in order to meet power benchmarks for HLS designs.

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For additional numbers, click here.

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