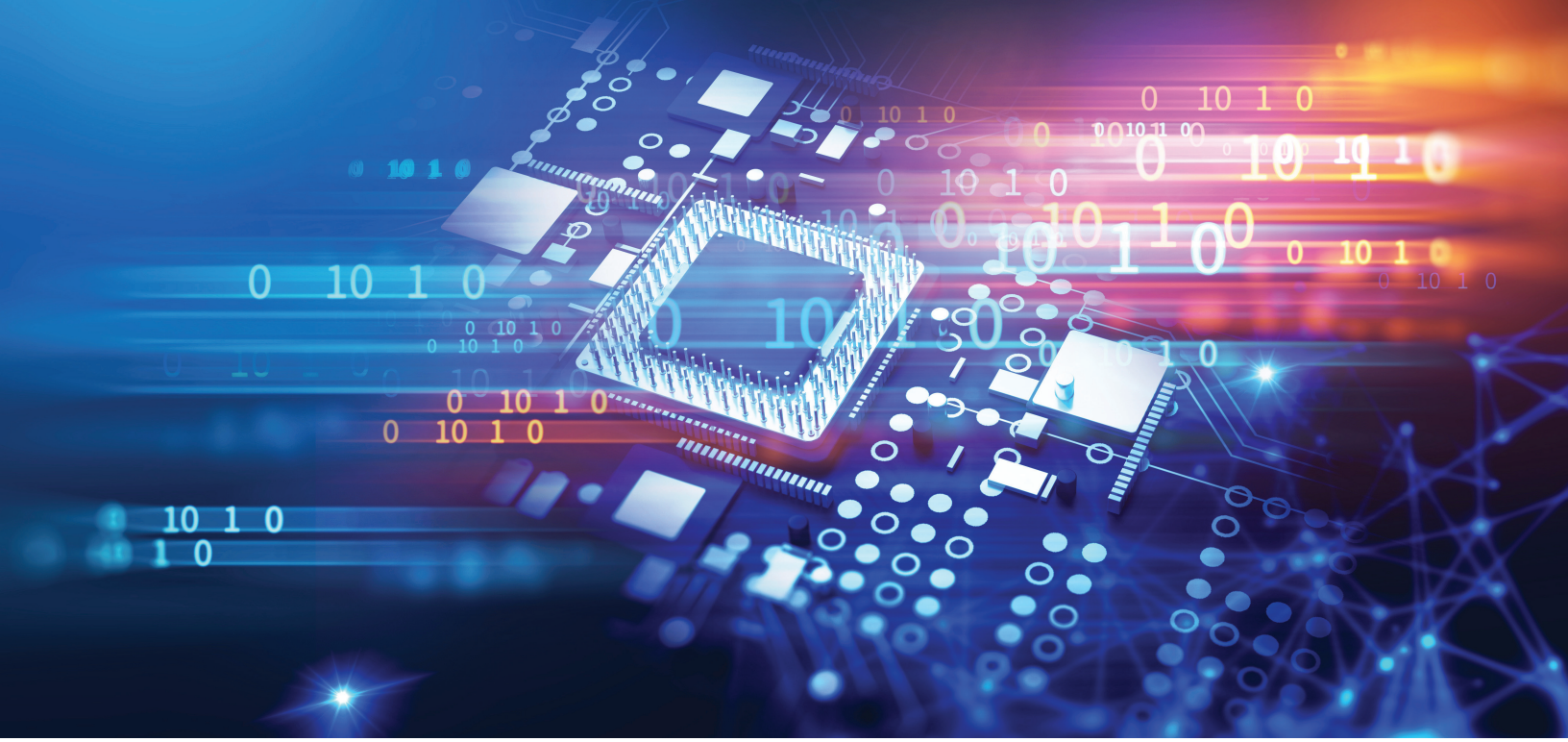
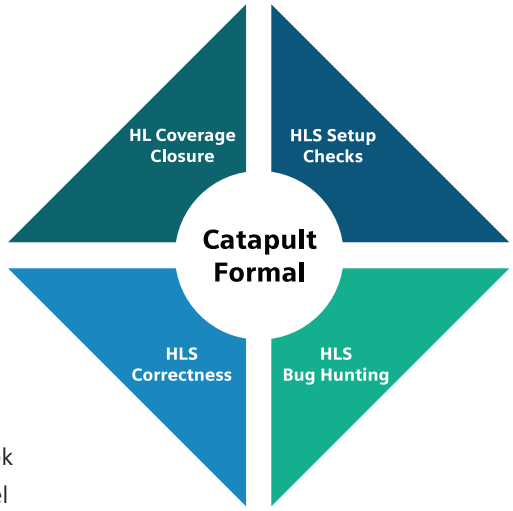


SIEMENS DIGITAL INDUSTRIES SOFTWARE

Catapult Formal

Delivering an efficient approach to high-level design and verification closure



Benefits

- Automatic setup and execution of formal analysis when using Catapult HLS
- Immediately identify mistakes, ambiguities, and other design issues
- Locate user constraint problems early in the High-Level Synthesis design and verification process
- Enable C-level verification and coverage flows across HL and RTL languages, even with timing and interfaces difference
- Friction-free process to build and verify hardware accelerators for optimal implementation with plug-and-play integration into existing RTL design and verification flows

Summary

Catapult™ Formal software adheres to the Catapult HLS Verification methodology that enables engineers to enhance their processes for accelerator IP design and verification as they seek an efficient approach to High-Level (HL) design and verification closure. C-level design benefits from high test coverage of the C model. Catapult Formal provides analysis of actual coverage by user test programs and identifies solutions to fill coverage gaps. Catapult Formal ensures that synthesis results are functionally equivalent to the original C/HL description and provides directed formal checks for specific synthesis implementations (i.e., FIFOs and handshakes) not present in the HL model. A variety of formal analysis and property checks can be selected with no learning curve and instant productivity. Catapult Formal expands your RTL test coverage beyond simulation alone.

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Catapult Formal Introduction

Catapult Formal is a suite of HL-targeted apps that adds confidence and checks implementation correctness. Catapult Formal is a plug-in that is compatible with existing RTL and UVM flows enabled by a suite of Catapult High-Level Synthesis (HLS) products, methodology and base-class libraries. The Catapult HLS system provides options and settings for the appropriate formal analysis. Some checks are for equivalence, and some are verification of the user constraints for synthesis. Catapult Formal also provides options and settings for appropriate formal analysis.

Capabilities

Users can enhance HL source coverage and correctness by applying property checks to the source and collecting coverage metrics from the HL source testbench. The HL coverage analysis can exclude unwanted system overhead code and provide witness waveforms for reachable coverage holes. Users can enhance the HL inputs, thereby gaining speed and efficiency in post-synthesis RTL closure.

User-provided constraints for HL synthesis can greatly improve area and throughput for memory implementations. Catapult Formal can verify that the original HL source intent and data flows are not violated by these user constraints. Most importantly, formal analysis can catch these functional errors early in the flow for maximum efficiency.

Catapult Formal has apps to validate the correctness of handshake logic inserted by synthesis to manage streaming data. Low-power designs insert logic to detect the idle times when data is exhausted. Catapult Formal apps evaluate the system for idle flag correctness, FIFO handshakes, and stalling.

At the core of Catapult Formal is a set of solvers which can be automatically configured for an equivalence check of C-level or RTL sources versus the synthesis RTL implementation. This powerful tool requires no user test bench and is set up and launched by the Catapult HLS system. Leaf module comparisons are supported for a bottom-up verification flow for efficiency, and multiple leaves of a design-unit are queued for successive or parallel runs. The principals of fast fault detection are applied with bounded, bug-hunt and path-by-path analysis options. High level equivalence check is one element of a HL verification plan which includes high coverage simulation and directed testing of the corners created by the synthesis architecture and processes.

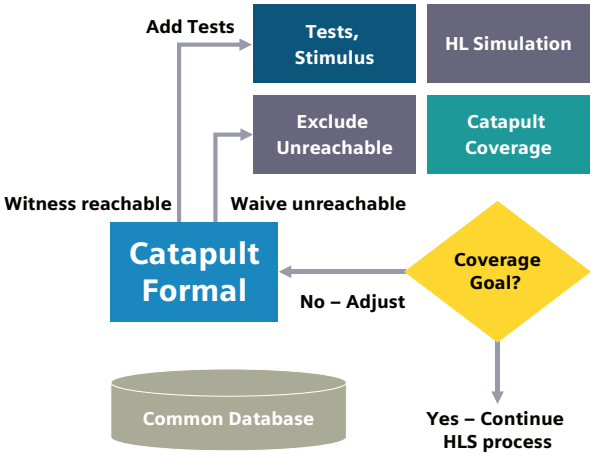
HLS verification process

- HL-centric apps for confidence and correctness
- Plug-in with existing RTL flows and UVM principles
- Find mistakes, ambiguities and undesirable design issues and user constraints early in the process
- Enables verification and coverage closure flows despite any language and/or timing differences
- Used by HLS designers and verification teams to detect differences with bug hunting

Verification efficiency

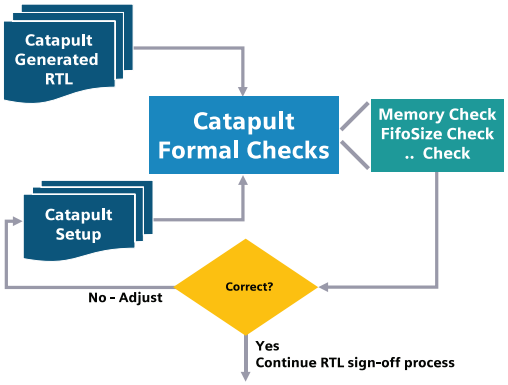
Close coverage before synthesis

- Reachability analysis
  - Waive unreachable coverage points
  - Witness reachable coverage points for simulation replay, greater insight
- Catapult Coverage integration



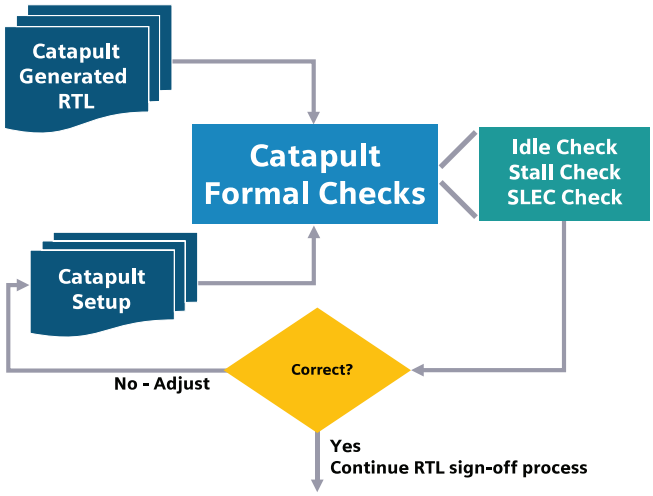
Early detection of mistakes, setup problems

- Check memory sequential dependency
- Check FIFO depths between blocks



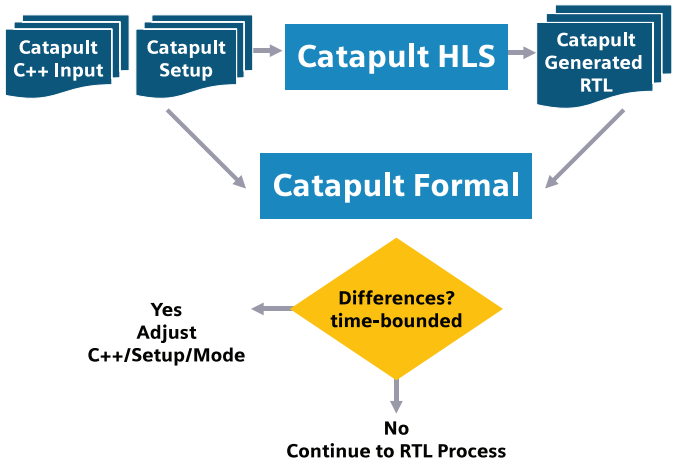
Early detection of implementation differences

- Inferred mistakes, constraints problems
- Correctness of Idle signal logic
- Correctness, worst-case stall buffer size



Early detection of behavioral differences

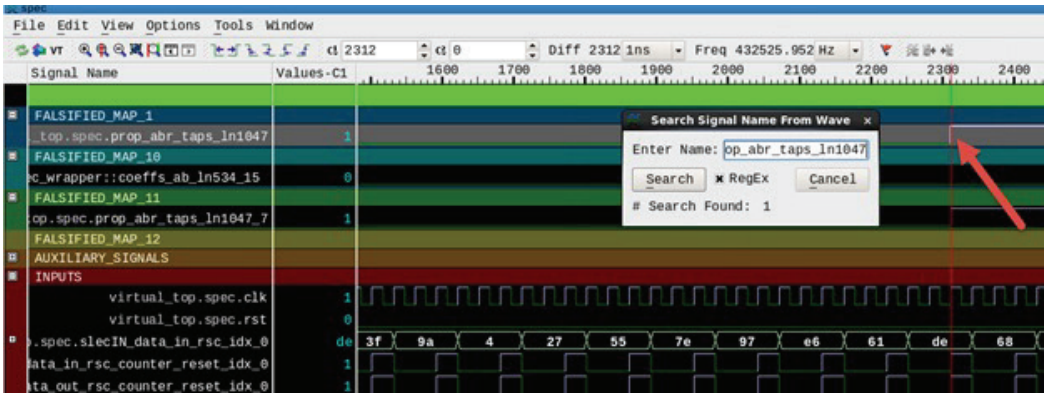
- Search for differences between HLS model, HLS setup and HLS created RTL
- Formal comparisons using guided methodology for specification/implementation checking
- Bug hunting checking for fast results
- Bounded checking limits transaction counts
- Path-by-path checking available
- Case splitting and grid computing is supported



Debug support

Catapult Formal interfaces to Siemens EDA Questa Simulation, Formal and Coverage tools as well as major third-party EDA simulation and wave display tools. Counter examples of falsifications or assertions are automatically generated, and an executable test bench is created. Tutorial exercises are provided in the installation.

View_waveforms: Debugging Falsifications



Supported platforms and programs

Platforms: Linux OS RHEL6, 7, 8 and compatible CentOS

Programs: Siemens EDA Questa Sim, Formal, and Visualizer. Synopsys VCS and Verdi

Siemens Digital Industries Software

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1 800 498 5351

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00 800 70002222

Asia-Pacific
001 800 03061910

For additional numbers, click here.

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