

**DIGITAL INDUSTRIES SOFTWARE**

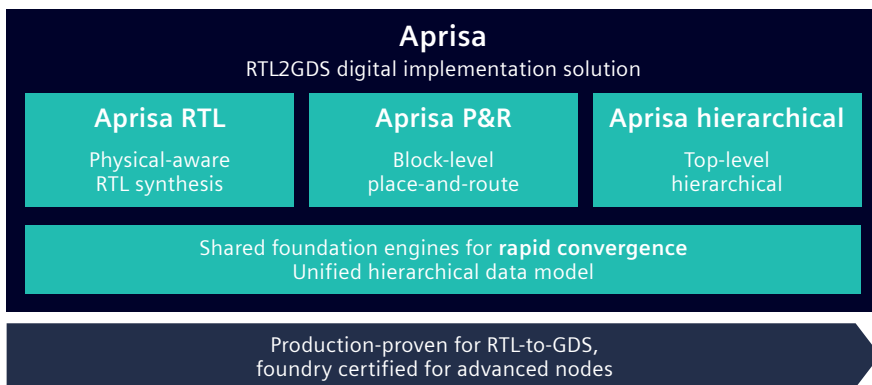
# Aprisa RTL-to-GDS digital implementation solution

**Benefits**

- 3X faster time to design closure
- 10% better PPA
- Strongest correlation to DRC and STA signoff tools, minimizing time to signoff closure
- Rapid ramp-up to productivity and ease of use, with out-of-the-box reference flows and built-in AI technologies

**Summary**

RTL-to-GDS digital implementation is an essential step for digital integrated circuit design. With increasing design complexity and a challenging time-to-market, this step often becomes a bottleneck in achieving optimal design performance, power and area (PPA) within the available time and resources. Aprisa™, the complete RTL-to-GDS digital implementation solution from Siemens EDA,



Aprisa digital implementation solution architecture.

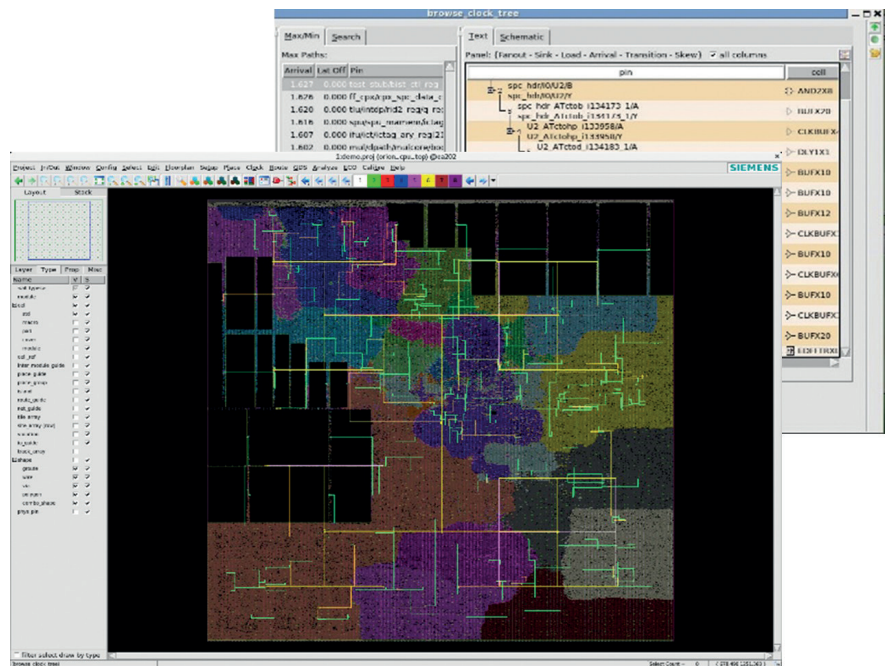
**Features**

- Complete support for RTL-to-GDS digital implementation and optimization, including RTL synthesis, placement, clock-tree synthesis, and route
- Detail-route-centric architecture with unified hierarchical data model and shared foundation engines
- Physical-aware RTL synthesis
- PowerFirst mode optimizations for power-sensitive designs
- Patented In-Hierarchy-Optimization (iHO) for fast top-level timing closure
- Advanced node ready and certified by leading foundries
- Interoperability with most industry's EDA tools
- 10x Productivity boost with Aprisa AI

provides 3X faster time to design closure and 10% better PPA to help design teams reach their goals. With exceptional quality-of-results out-of-the-box, and advanced AI technologies, Aprisa helps to maximize engineering productivity. This digital implementation solution interoperates with most of the industry's EDA tools through standard input/output file formats. Aprisa is certified by leading foundries and is being deployed to implement designs utilizing the most advanced technology nodes.

**10% better design PPA**

Every design has its unique set of performance, power, and area targets. Aprisa offers different modes to choose from, to perform metric focused optimizations. This provides engineering teams with flexible tradeoffs to achieve competitive design PPA. As an example, the PowerFirst mode in Aprisa enables designers to start implementation based on the best power attainable for a given design, and drive towards convergence with best performance.



User friendly Aprisa GUI showing a custom CTS for HPC designs.

**3x faster time to design closure**

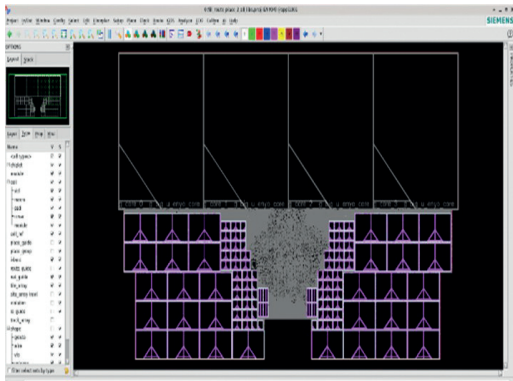
Aprisa shortens the time to design closure and tapeout, while dramatically improving the PPA predictability and correlation. Aprisa's detailed-route-centric architecture includes a unified database, data model and shared foundation engines, and maintains detailed routing topologies of critical nets throughout the RTL-to-GDS flow. This technology, combined with Aprisa's native physical-aware RTL synthesis, reduces the number of design iterations, thereby achieving faster design closure.

### Quality of signoff correlation

Aprisa's correlation has been proven to match very closely with that of the industry's standard signoff tools. This further improves the design PPA by eliminating the need for an extra guard band. It also reduces the number of Engineering Change Order (ECO) iterations, resulting in a shorter time to signoff closure.

### Fast top-level timing closure

Aprisa reduces the effort required to achieve top-level timing closure from weeks to days. Aprisa's patented in-Hierarchy-Optimization technology leverages its unified hierarchical data model to offer fast top-level timing closure without timing re-budgeting or hierarchy flattening.



Top-level timing closure with in-Hierarchy-Optimization for a quad-core CPU.

### Extensive Foundry support

Aprisa collaborates with leading foundries on tool certification for advanced nodes. Aprisa enables designers to have access to certified technology collaterals and tool support for successful tapeouts, at both cutting edge and mature nodes from semiconductor foundries.

### Interoperability with EDA tools

Aprisa is interoperable with semiconductor industry's EDA tools through the support of standard data inputs and outputs, such as Verilog, SDC, LEF/DEF, .lib, UPF/CPF, and GDSII. In addition, Aprisa is well integrated with all Siemens digital solutions, such as Tessent and Calibre, for complete and seamless digital flow support.

### 10x Productivity with Aprisa AI

By adopting artificial intelligence (AI) technologies throughout the RTL-to-GDS digital implementation design flow, Aprisa addresses the productivity gap the semiconductor industry is facing. With Aprisa AI, RTL-to-GDS digital implementation teams can benefit from a 10X productivity boost, 3X faster time to production, and 10% better design PPA.

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