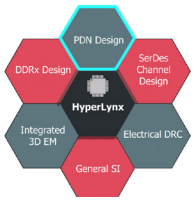
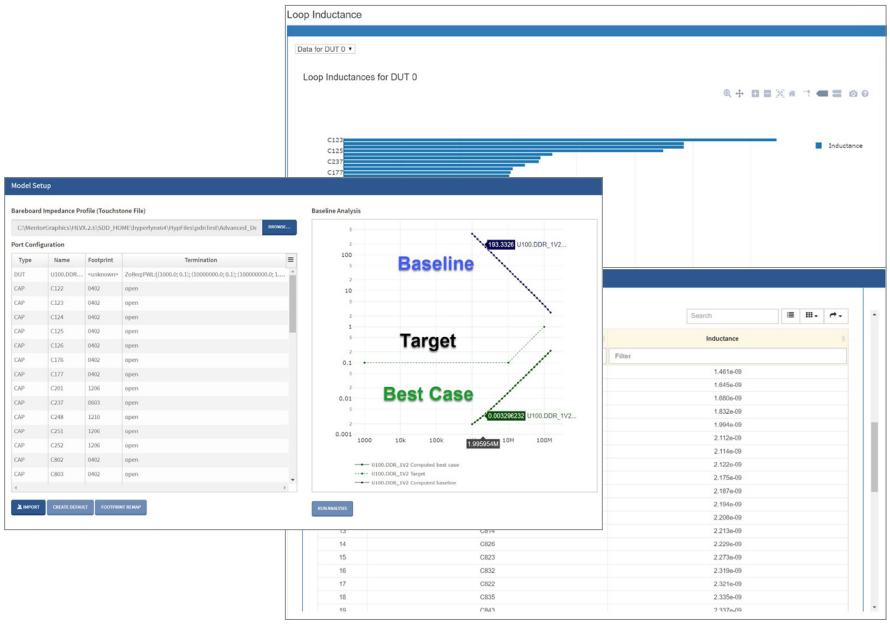


PDN Decoupling Optimizer

Reduce costs while ensuring performance

DATASHEET



The HyperLynx PDN Decoupling Optimizer automatically determines the optimum configuration of decoupling capacitors based on your design's unique impedance requirements.

KEY CAPABILITIES

- Cost-reduce existing designs – identify capacitors that can be removed without affecting PDN performance
- Optimizes PDN performance to meet impedance requirements
- Integrates with HyperLynx LineSim to perform interactive "what-if" trial layouts and optimization
- Integrated 3D EM solvers provide fast, accurate modeling of PDN behavior
- Automated workflow with HyperLynx's industry-renowned ease of use
- Works with all major PCB layout and routing applications

Overview

Designing a PCB Power Distribution Network (PDN) is a complex problem. The physical limitations of PCB and IC package construction mean that power delivered from the PCB to IC power pins typically tops out at ~150 MHz, with a combination of IC package and on-die decoupling supplying power above that point. Below 150 MHz, the PCB PDN must provide a very low impedance path (typically 25 milliohms or less) between the VRM and the IC's power pins. Providing a path with this target impedance from the VRM to IC power pins all over the board requires a spatial network of different value capacitors, each serving power needs for a particular frequency range within a particular area. Each unique capacitor type has a radii of effectiveness based on its fan out routing and the power planes it connects to, and each IC type will have its own current draw vs. frequency characteristics, with its own set of power impedance vs. frequency requirements. All these issues combine to make good PDN design a complicated, multi-dimensional problem.

The realities of modern business and PCB design also mean that boards have to be designed quickly while still ensuring they are ready for high-volume production. Product lifecycles are too short; missing a launch window due to an extended design cycle may mean lost profits or market position that cannot be recovered. A product that launches on time but fails intermittently in the field can be worse than a product that doesn't launch at all. Product lifetimes are too short to recall and rework products, and a company that burns a customer once may never earn their trust again.

The traditional solution is simple – overdesign the PDN and "play it safe", then depopulate capacitors as time permits during lab testing. Most PDN designs have many more capacitors than they need as a result. This drives up design costs in subtle ways – besides the cost of the capacitors themselves, there's the board space they require, the time to design them in, a possible increase in PCB layer count, increased assembly costs and the increased possibility of failure due to their presence. That's still better than missing a launch window, but leaves lots of room for improvement.

The HyperLynx PDN Decoupling Optimizer can quickly cost reduce an existing without requiring layout changes, by identifying existing capacitor locations than can be no-populated or swapped with other capacitors that have the same footprint. It's just as quick and effective for new designs, allowing the design engineer to mock up and optimize a decoupling strategy graphically, without requiring design changes from the layout designer during analysis. Once a layout strategy is defined, the designer passes that information back to layout for implementation and subsequent verification.

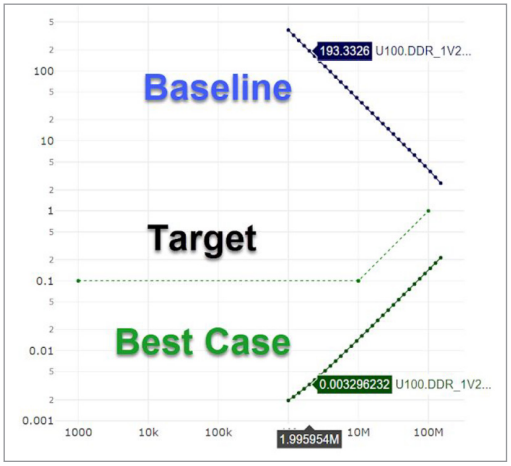
PDN Optimization Flow

Optimization occurs in stages, with each stage identifying specific basic issues and ensuring readiness for the next stage. This accelerates your design cycle by resolving issues as early as possible and performing deep, compute-intensive runs only when necessary. PDN optimization stages include:

- Baseline analysis
- Expert-based PDN synthesis
- PDN optimization
- Export of optimization results

Baseline Analysis

Baseline analysis defines impedance requirements for critical components and computes PDN behavior using ideal capacitors. This help ensures a PDN solution is possible before running more detailed analysis. If impedance targets cannot be met with ideal capacitors, either capacitor mounting needs to improve, more capacitors are needed or the requirements may be incorrect. Baseline analysis produces a report that plots PDN performance and details loop inductance for each capacitor to highlight potential problem areas.



Expert-Based Synthesizers

This stage employs a set of Expert-based synthesis algorithms that use different methods to drive decoupling capacitor selection and meet impedance requirements. Each algorithm runs iteratively, adding capacitors to meet the impedance target using strategies as listed below (click on the algorithm name to see it in action):

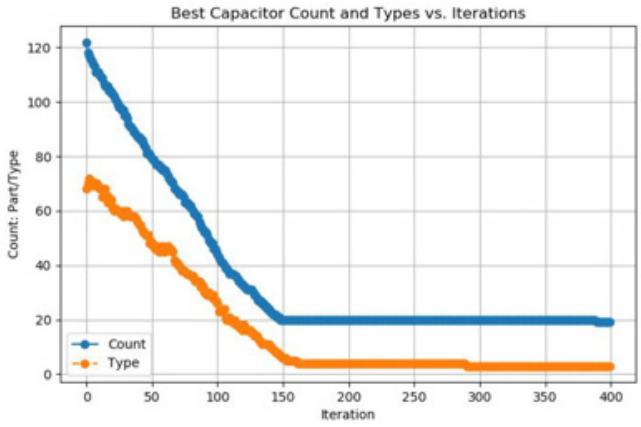
- Stomp Peaks – Targets frequency where Z0 is currently worst
- Bigger is Better - Places largest capacitor available
- High to Low – Targets highest frequency where Z0 > target
- Low to High – Targets lowest frequency where Z0 > target
- Ends In – Targets ends of frequency range where Z0 > target
- Center Out – Targets middle of range where Z0 > target

This produces a set of decoupling configurations, that can be used as-is or fed to the next stage for further optimization.

PDN Optimizer

The HyperLynx PDN Decoupling Optimizer uses an accelerated genetic optimization technique to find solutions that best meet impedance requirements while minimizing total design costs. This is a form of deep optimization that changes fairly quickly at first and then settles slowly. You control the number of generations in the process to control the tradeoff between optimization quality and run time.

You can define criteria that drive the optimization process, such as individual component costs or a cost criteria associated with adding another capacitor type to the mix. This helps you optimize the real costs associated with manufacturing your design.



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Export Optimization Results

Once optimization is complete, HyperLynx generates a report identifying capacitor locations and values. If you're optimizing an existing layout, you can "no populate" or swap part types to improve PDN performance and reduce costs. HyperLynx limits part swaps to capacitors with the same footprint to ensure a capacitor can be swapped without design rework. To further reduce costs or reclaim valuable board space, unused capacitors can be deleted from the design entirely and their space used for other purposes.

Supported PCB Layout Systems

- Tightly integrated with Mentor Graphics Xpedition™, PADS Professional® and PADS®
- Altium Designer (through ODB++)
- Cadence Allegro and OrCAD Layout tools
- Zuken CR Series

For the latest product information, call us or visit: www.mentor.com/pcb

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