HyperLynx
SERDES Analysis

DATASHEET

Overview

Beyond the design-specific technical challenges that are associated with designing and analyzing a Serialization – Deserialization (SERDES) interconnect, hardware engineers face industry-related complexities. For example, unlike the relative simplicity of a few double data rate (DDRx) specifications, there are more than 100 unique SERDES specifications. For printed circuit board (PCB) designs that contain multiple SERDES protocols, the lack of knowledge transferred between protocols means interconnect analysis has to start from scratch for every protocol.

HyperLynx® contains SERDES-specific functionality such as:

1. Intelligent, automatic channel extraction
2. Interface-level channel compliance verification
3. Pre-layout design exploration.

Together, these automate SERDES channel analysis while retaining the accuracy needed for these very high frequency interconnects.

FEATURES AND BENEFITS

- Fully automatic channel decomposition and modeling
- Embedded EM expertise
- Return-path aware, automatic 3D area creation
- Topology-specific automatic port creation, boundary conditions, meshing, and 3D field solver settings
- Tolerance-based 3D area pattern matching
- Embedded protocol domain expertise
- Support for Ethernet, OIF-CEI, Fibre Channel, PCI Express, JCOM, USB 3.1 protocols
- Protocol-compliant Tx/Rx models
- Comprehensive HTML reports
- Equalization optimization using CTLE, FFE, and DFE
- Template-based 3D structure synthesis

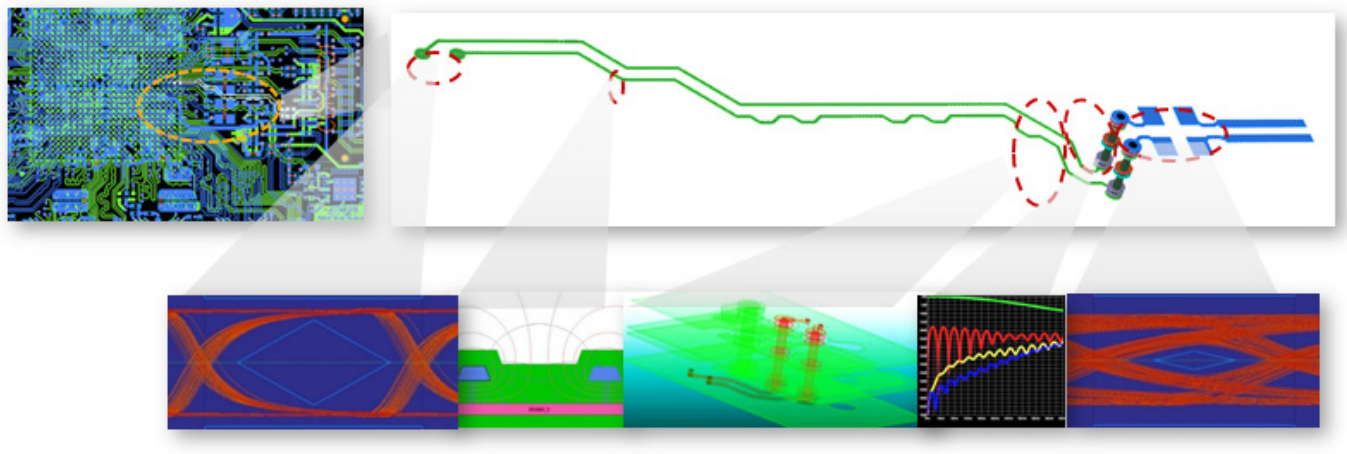

Figure 1: SERDES channel decomposition and modeling

SERDES Channel Analysis

The typical channel extraction and modeling approach involves:

1. Dividing the interconnect into sections that need to be modeled in 3D and 2D field solvers, respectively
2. Generating S-parameter models for the sections modeled with a 3D field solver
3. Reconnecting the S-parameter models from the 3D field solver with the 2D field-solver-modeled sections to represent the entire interconnect
4. Exporting an S-parameter model of the entire interconnect for frequency domain analysis or compliance verification.

The steps above are performed manually. As such, the process requires high attention to detail making it both time-consuming and error-prone (Figure 1). Further, it requires in-depth electromagnetic (EM) expertise to ensure that the resulting model(s) (from step 2, above) is accurate.

For example, aggressively dividing (or cropping) the interconnect (step 1) without understanding where the return path exists yields an inaccurate S-parameter model (step 2). Conversely, a conservative crop of the interconnect increases simulation run time and memory consumption.

Further, creating ports that are valid up to a very high frequency (step 2) or specifying the appropriate boundary condition to suppress reflections from the cropped edges (step 2) is not a trivial task.

Intelligent, Automatic Channel Extraction

HyperLynx automates the entire process above. After the SERDES nets in the design are identified, the process is executed with the push of a single button.

HyperLynx identifies which parts of the net should be modeled in a 3D field solver based on the design (Figure 2). Port creation, boundary conditions, meshing settings, etc. are specified based on the class of problem being solved, while generating accurate results in a timely manner.

The EM expertise needed to accurately model the problem is embedded within the software. The resulting S-parameter model can be used for frequency-domain analysis or compliance verification (see next section). Further, if the same PCB structure, such as a via pattern, is present in other parts of the design, the S-parameter model from the initial analysis can be automatically reused, which greatly accelerates subsequent analyses.

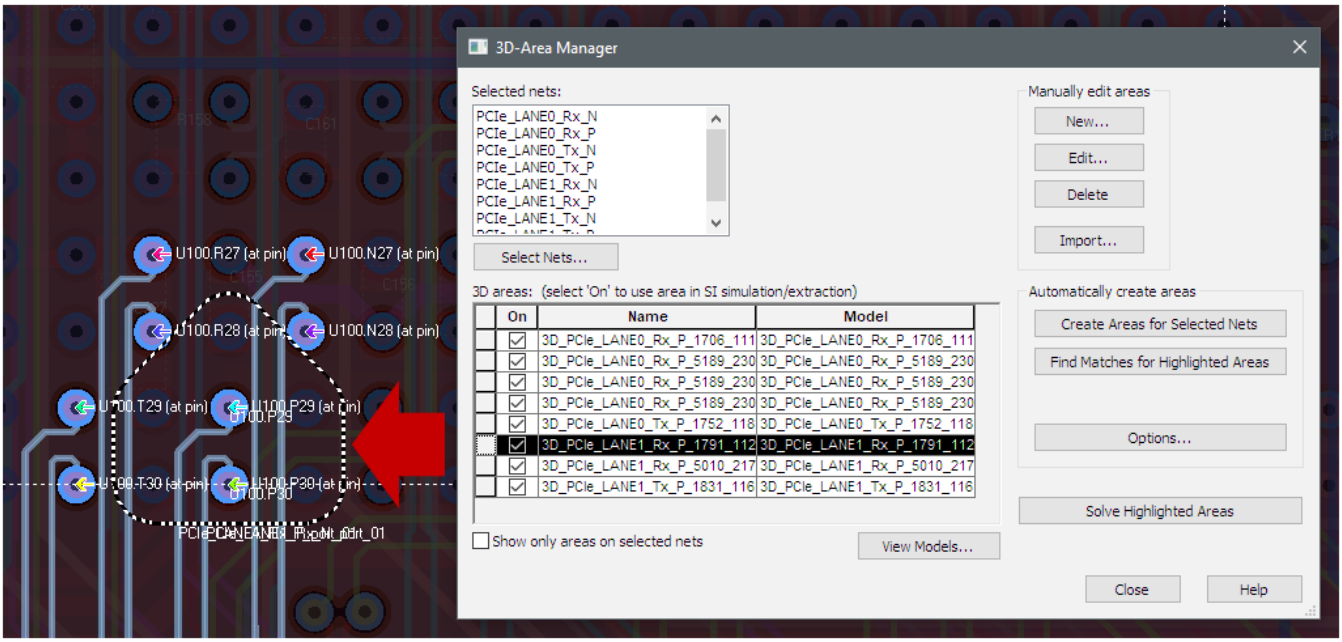

Figure 2: 3D area automatically created based on the available return path

Interface-level Channel Compliance Verification

Channel compliance verification is not a trivial task. The hardware engineer needs to understand the specification, which can be 1000 pages long (PCI Express Gen 3 and Gen 4). The specifications, which are not free or easily accessible, are written by compliance bodies and are inconsistent across protocols. For example, jitter is specified in different ways in the PCI Express and IBIS-AMI specifications. Given design-cycle pressures, hardware engineers do not have the time or required training to properly understand the detailed specification(s).

With HyperLynx, the protocol domain expertise needed to evaluate an interconnect is embedded within the tool itself (Figure 3).

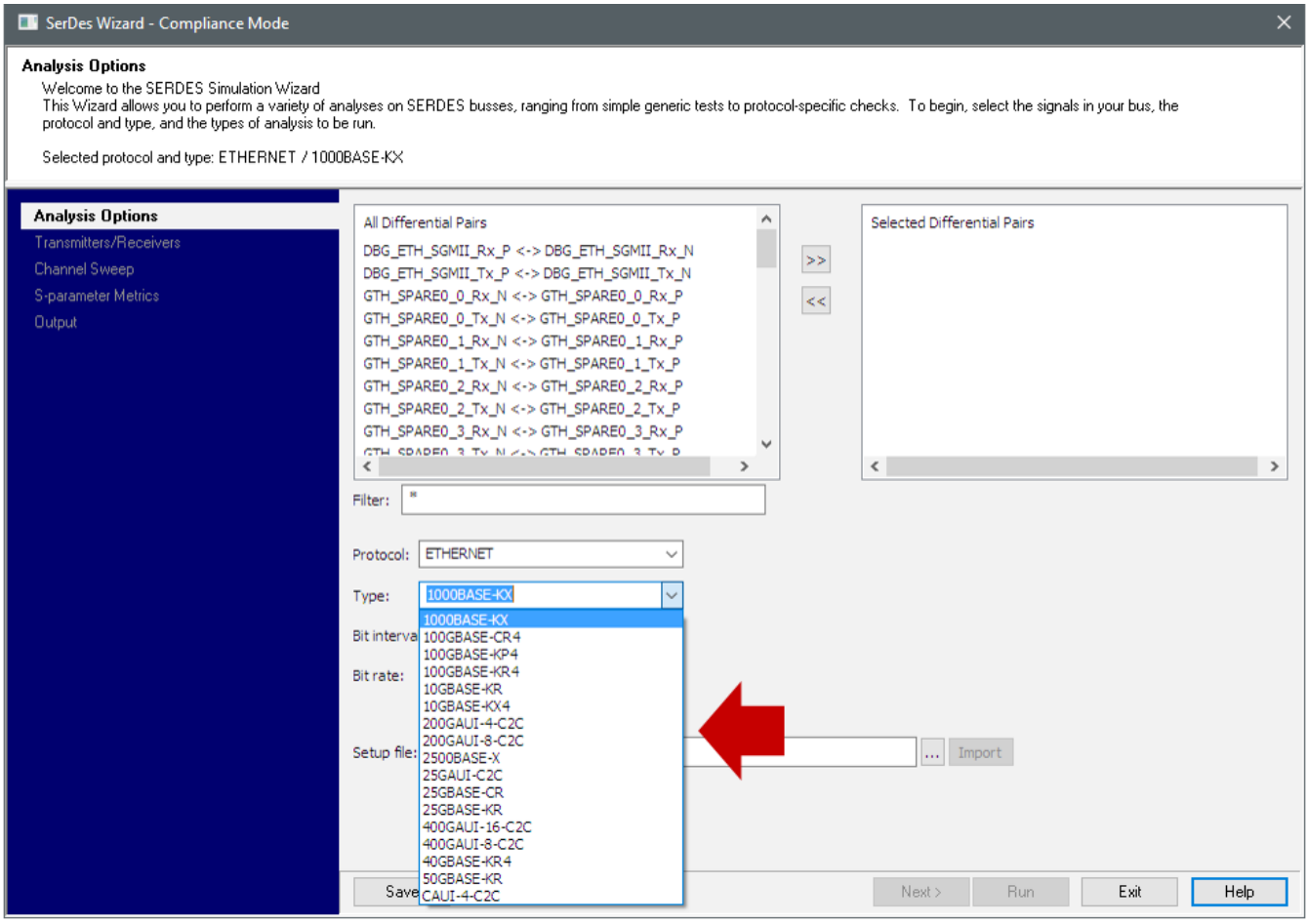

Figure 3: Protocol domain expertise for verifying interconnects is built into HyperLynx

Support exists for channel operating margin (COM) based methods to evaluate interconnects for adherence to multiple protocols (Figure 4).

Bit rate	ANSI	Ethernet	JCOM	OIF-CEI	PCI Express	USB
1 - 5 Gbps		**1000BASE-KX** **2500BASE-X** **10GBASE-KX4**			**PCIe Gen1 -2.5GBps** **PCIe Gen2 -5GBps**	**USB3.1 -Gen1 -5Gbps**
5 - 10 Gbps		10GBASE-KR 40GBASE-KR4			PCIe Gen3 -8GBps	USB3.1 -Gen2 -10Gbps
10 - 25 Gbps	**ANSI-FC-PI-6**	**100GBASE-KP4** **CAUI-4-C2C**			**PCIe Gen4 -16GBps**	
25 - 50 Gbps		25GAUI-C2C 25GBASE-CR 25GBASE-KR 50GBASE-KR 50GBASE-CR 200GAUI-4-C2C 200GAUI-8-C2C 400GAUI-8-C2C 400GAUI-16-C2C 100GBASE-KR4 100GBASE-CR4	JESD204C	CEI-25G-LR CEI-28G-MR CEI-28G-SR CEI-56G-LR-PAM4 CEI-56G-MR-PAM4 CEI-56G-XSR-PAM4	PCIe Gen5 -32GBps	
> 50 Gbps				**CEI-56G-USR-NRZ**		

Figure 4: Supported protocols for channel compliance verification

The hardware engineer can use built-in protocol-compliant driver and receiver models to evaluate the entire interconnect, thereby eliminating the need for IBIS-AMI models.

The use of behavioral models allows channel compliance verification to run much faster than when IBIS-AMI models are used. HyperLynx helps identify optimum equalization settings based on protocol reference architecture and constraints such as decision feedback equalization (DFE), continuous time linear equalization (CTLE), etc. Channel optimization can be performed in both the pre-layout analysis and post-layout screening phases. HTML reports that contain the channel compliance verification results are created, which allows for easy sharing.

Pre-layout Design Exploration and Optimization

Most analysis for SERDES channels is performed in the pre-layout phase of the PCB design cycle. It involves creating a default geometry/configuration, such as for a via pattern, and then modifying it to optimize the structure. Given the number of parameters that can be edited and the various values that they can assume, the number of topology configurations is endless.

HyperLynx uses a template-based approach that helps a hardware engineer optimize a specific design geometry (Figure 5). Templates for structures such as differential vias, ball grid array (BGA) break-outs and break-ins, series blocking capacitor mountings, etc., along with their associated parameters, can be modified.

The parameter values can be swept in various combinations as a "system of experiments" and measurement constraints can be applied to identify those configurations that satisfy specific criteria. The resulting configuration(s) and its associated S-parameter model(s) can then be used for further time- or frequency-domain analysis.

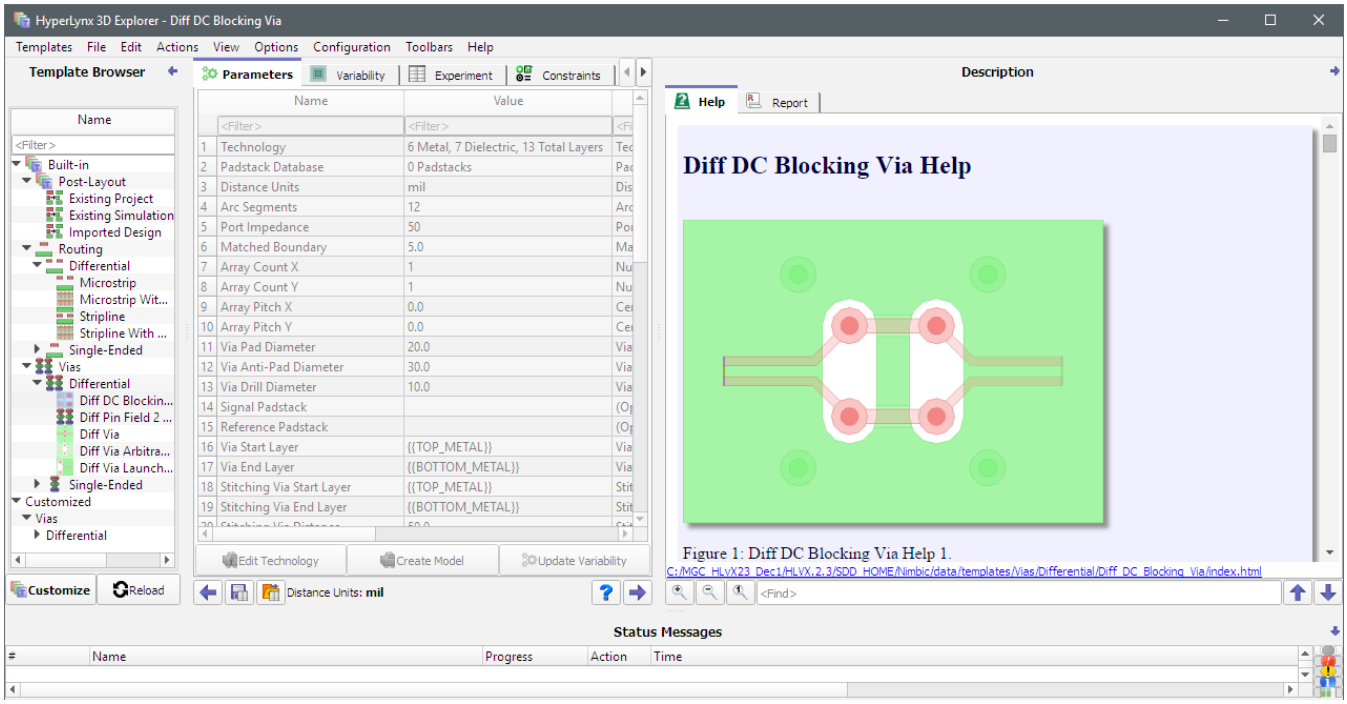

Figure 5: Template for a differential DC blocking via configuration

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Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000
sales_info@mentor.com

Silicon Valley
Mentor Graphics Corporation
46871 Bayside Parkway
Fremont, CA 94538 USA
Phone: 510.354.7400
Fax: 510.354.7467

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
11F, No. 120, Section 2,
Gongdao 5th Road
HsinChu City 300,
Taiwan, ROC
Phone: 886.3.513.1000
Fax: 886.3.573.4734

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Trust Tower
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: +81.3.5488.3033
Fax: +81.3.5488.3004

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